Service Repair Documentation Level 3 – SXG75



Release	Date	Department	Notes to change	
1.0	24.01.2006	BenQ Mobile CC S CES	New document	

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1 Instruction

This Service Repair Documentation is intended to carry out repairs on BenQ Mobile repair level 3. The described failures shall be repaired in BenQ Mobile authorized local workshops only.

All repairs has to be carried out in an ESD protected environment and with ESD protected equipment/tools. For all activities the international ESD regulations has to be considered.

Assembling/disassembling has to be done according to the latest SXG75 Level 2 repair documentation. It has to be ensured that each repaired mobile phone is checked according to the latest released General Test Instruction document (both documents are available in the technical support section of the C-market).

Check at least weekly C-market for updates and consider all SXG75 related Customer Care Information and Repair Information which are relevant for the SXG75.

SXG75 partnumber on IMEI label: S30880-S8900-#xxx

, while # can be any letter (A-Z) and xxx can be any number from 100, 101, 102....

Scrap handling: All scrap informations given in this manual are related to the SCRAP-Rules and instructions.

Attention: Consider the new "LEAD-FREE" soldering rules (available in the communication market) and avoid excessive heat.

If you do have any questions regarding the repair procedures or spare parts do not hesitate to contact our technical support team in Kamp-Lintfort, Germany:

Tel.: +49 2842 95 4666 Fax: +49 2842 95 4302 e-mail: st-support@benq.com

2 List of available spare parts

(according to Component Matrix V1.03 - check C-market for updates)

Component	Ordernumber	Description
V101	L50640-D4060-D670	DISDIODE DUAL ESD-PROTECTION SOT23
V200	L50630-C1101-D670	DISTRANS SI1555DL
N200	L50645-K280-Y337	IC FEM LMSP43MA-288TEMP GSM UMTS SMD
Z203	L50645-K280-Y323	FILTER DUPLEX WCDMA
Z200	L50645-K280-Y331	FILT SAW RX PCS1900MHZ B7846
Z201	L50645-K280-Y332	FILT SAW RX DCS1800MHZ B7844
Z202	L50645-K280-Y333	FILT SAW RX GSM900MHZ B7837
D500	L50620-L6165-D670	IC TELEC TRANSCIEVER RTR6250 QFN56
N300	Not defined yet	IC MODUL PA PF0814 (PA-Type3) PB Free
V300	L50630-C1101-D670	DISTRANS SI1555DL
Z300	L50645-G100-Y108	OSCOSCI TXVCO 824-1910MHZ SMD
Z400	L50645-K260-Y93	ISOLATOR 1920MHZ-1980MHZ SMD
D400	L50651-Z2002-A66	IC TELEC ACPM-7881 SMD
V400	L50630-C1101-D670	DISTRANS SI1555DL
Z402	L50697-F5005-F88	IC TELEC RF-DETECTOR SOT23-6L
Z401	L50645-K280-Y314	FILT SAW UMTS2100 1950MHZ B7754
Z602	L50697-F5020-F34	EPCOS SAW LOW-LOSS-FILTER 2140,0MHZ LG02
X600	L36334-Z97-C334	CONNECTOR COAX SOCKET SWITCHED
Z600	L50645-K280-Y293	FILTER SAW AGPS 1575,42MHZ B7840 SMD
Z601	L50645-K280-Y304	FILSAW 1575,42 MHZ B7829 SMD
N600	L50620-L6166-D670	IC TELEC RECEIVER GPS UMTS RFR6250 QFN48
N700	L50610-U6197-D670	IC ANA STEREO-AMPLIFIER TS4975 CSP12
D800	L50620-L6164-D670	IC TELEC MSM6250 CSP409
Z1000	L50645-G200-Y27	OSCOSCI VCTCXO 19.2MHZ SMD
V1100	L50640-C3008-D670	DISTRANS PNP 0,5A 30V SOT89
V1102	L50630-C3007-D670	DISTRANS P-CH SI2333DS FDN306P SOT23
N1100	L50610-C6181-D670	IC VOLTAGE REG.TPS73601DRBR SMD ADJUSTA
V1101	L50640-D5086-D670	DISDIODE RB551V-30 PMEG3005AEA SOD323
Z1200	L50640-U6064-D670	FILTER EMI (Fi-Type7) PB Free
Z1201	L50610-C6179-D670	IC SPDT SWITCH DUAL MAX4717EBC+T UCSP12
V1303	L50640-D4043-D670	DIODENARRAY ESDA6V
Z1300	L50645-F102-Y42	OSCCRYST 32,768KHZ 7,0PF 30PPM SMD LF
N1300	L50645-J4681-Y57	IC POWER-MANAGMENT PM6650
V1301	L50640-D5086-D670	DISDIODE RB551V-30 PMEG3005AEA SOD323
D1300	L50610-C6183-D670	IC LOGIC NAND 74LVC1G00 SOT886
V1302	L50640-D5086-D670	DISDIODE RB551V-30 PMEG3005AEA SOD323
V1300	L36840-D5076-D670	DIODE SOD323 (Di-Type7)
Z1600	L50645-K280-Y328	FIL BP 2,4GHZ SMD
N1600	L50610-L6155-D670	IC TRANSCEIVER BLUETOOTH BCM2004 SMD
D1800	L50620-L6150-D670	IC TELEC TEA5764HN
V1800	L36840-D61-D670	DIODE 1SV305 (Di-Type4)

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V1801	L36840-D61-D670	DIODE 1SV305 (Di-Type4)
V1900	L36840-C4057-D670	TRANSISTOR EMD12 EMT6 (Tra-Type8)
N1900	L50610-C6152-D670	IC ANA REG 2*2,85V 150MA USMD8 LP3986T
D1900	L50610-B6198-D670	IC LOGIC BUFFER 74ALVC16244AZQLR VBGA LF
D1901	L50610-B6198-D670	IC LOGIC BUFFER 74ALVC16244AZQLR VBGA LF
V2000	L36840-C4014-D670	TRANSISTOR BC847BS BC846S (Tra-Type7)
D2100	L50610-B6134-D670	IC LOGIC NC7WZ126L8X MAC08A
V2101	L50640-C4060-D670	DIS TRANS ARRAY EMD9 EMT6
D2200	L50610-B6186-D670	IC LOGIC 2 INPUT AND NC7SZ08L6X
N2201	L50610-C6153-D670	IC ANA RE 2.9V USMD5 PB FREE
V2200	L36840-C4014-D670	TRANSISTOR BC847BS BC846S (Tra-Type7)
V1700	L50640-D5086-D670	DISDIODE RB551V-30 PMEG3005AEA SOD323

3 Required equipment for level **3**

- GSM-Tester (CMU200 or 4400S incl. options)
- PC, incl. monitor, keyboard and mouse
- USB boot cable (F30032-P465-A1)
- Troubleshooting frame SXG75
- Power supply
- Spectrum analyser
- Active RF-Probe incl. power supply
- Oscilloscope incl. probe
- RF-Connector (N<>SMA(f))
- Power supply cables
- Dongle (F30032-P28-A1). If USB-Dongle is used, a special driver for NT is required
- Soldering and BGA soldering equipment for lead free soldering.

Reference: Equipment recommendation (downloadable from the technical support page)

4 Required software for level 3

- Windows XP
- XFocus V2.06
- GRT V3.07
- Internet unblocking solution (JPICS)

5 Radio part

The RF section consists of three data capable transceivers and two further broadcast receivers. The first transceiver is an IMS UMTS 2100MHz 3G solution which realizes the conversion of the RF WCDMA signals from the antenna to the baseband and vice versa. The second transceiver is a GSM part which realizes the conversion of the GMSK-RF-signals from the antenna to the baseband and vice versa. The third transceiver is a Bluetooth type Personal Wireless LAN system. The first broadcast receiver is an RDS compliant FM radio solution. The second is a GPS receiver which is integrated into the UMTS receiver IC. The GPS software will allow assistance from a suitably enabled network (A-GPS); standalone operation without network assistance is also supported.

The GSM part supports triple band operation in the frequency ranges EGSM900, DCS1800, PCS1900 respectively supporting GPRS functionality up to multiclass 10. In the receiving direction, the RF signals are filtered and then directly down-converted and split into the I- and Q-component and led to the D/A-converter of the logic part. In the transmission direction, the GMSK-signal is generated in an Up Conversion Modulation Phase Locked Loop by modulation of the I- and Q-signals which are generated in the logic part. The high power Tx VCO is external to the RFIC. After that the signals are amplified in the power amplifier. The GSM transmitter and receiver are never active at the same time (TDMA system).

The Bluetooth solution is realized in a separate IC with an external SAW filter.

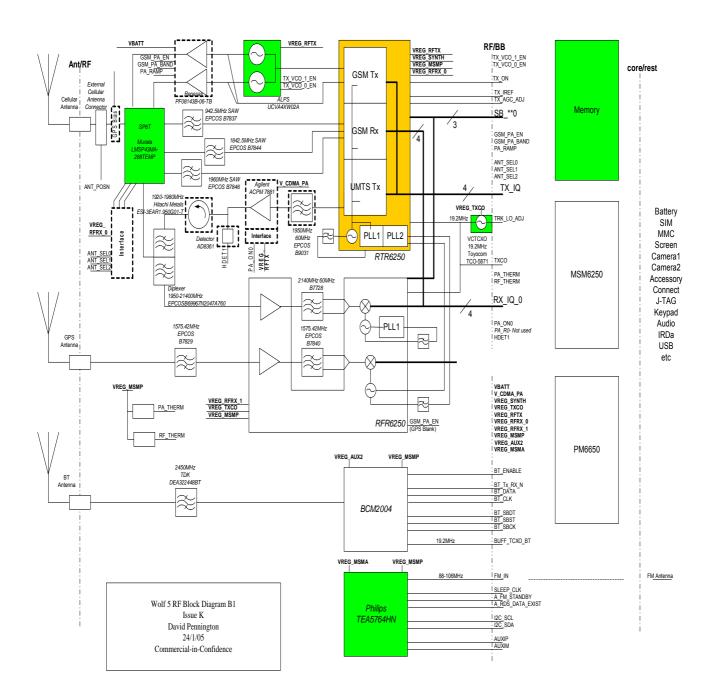
The GPS receiver is integrated into the UMTS receiver RFIC. Two stages of filtering are provided in front of and behind the LNA. The GPS down-conversion is a direct conversion system.

The FM radio solution is also realized in a separate IC.

The RF-circuit consists of the following components:

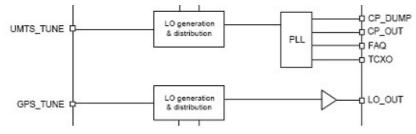
- Qualcomm chip set RTR6250 for GSM TX/ RX, UMTS TX, LO1, PLL for GPS LO
- Qualcomm chip set RFR6250 for UMTS RX, GPS RX, UMTS VCO, GPS VCO
- VCTCXO 19,2 MHz
- GSM TX VCO
- GSM PA module
- UMTS PA module
- UMTS duplexer and isolator
- BCM2004 Bluetooth IC
- FM radio

5.1 Block diagram RF part



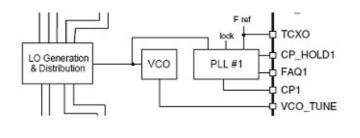
5.2 Receiver (RTR6250 and RFR6250)

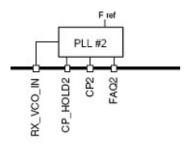
The RFR6250 has two VCOs. The first is for the UMTS direct conversion receiver. The second is for the GPS receiver and the PLL for this VCO is on the RTR6250 RFIC.



Block diagram RFR6250

The RTR6250 contains two PLLs, the first is used by the RTR for all GSM transceiver functions and for the UMTS TX LO generation. The second PLL is used to control the GPS VCO in the sister RFR6250 RFIC.



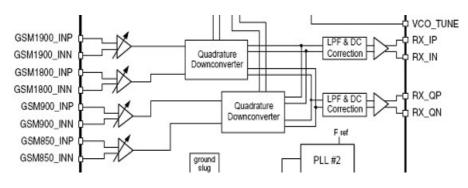


Block diagram RTR6250

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5.2.1 GSM RX

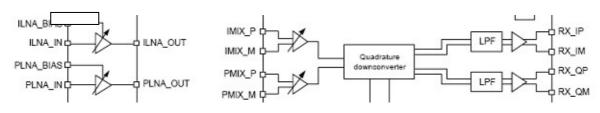
The GSM Receiver is a zero IF architecture with direct conversion by the IC. Although the IC provides four input paths, the GSM850 Receiver is not used in the SXG75.



Block diagram RTR6250

5.2.2 UMTS RX

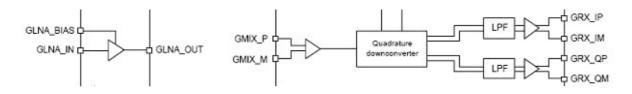
The RFR6250 provides an LNA and an output to allow further input filtering. The balanced signal is reconnected to the RFR6250 and down converted by the Zero IF Quadrature Downconverter. The UMTS 1900 RX path (PLNA, PMIX) is not used in the SXG75.



Block diagram RFR6250

5.2.3 GPS

The GPS path is similar to the UMTS path, but uses a LNA with higher amplification to compensate the DCS self blocking. The RFR6250 allows the GPS RX path to be switched off during GSM transmit pulses.



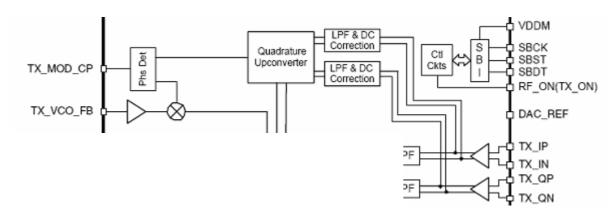
Block diagram RFR6250

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5.3 Transmitter

5.3.1 GSM TX modulation

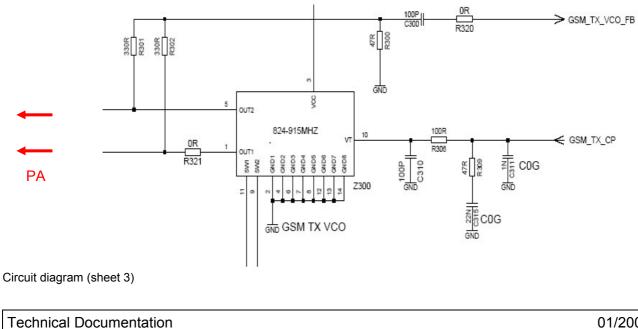
The GSM transmitter uses a Offset Phase Lock Loop Architecture. The high power VCO is external to the RTR6250. A feedback signal from the VCO is down-converted and the phase compared to that of an upconverted version of the IQ signals from the baseband. The control signal is filtered and passed to the high power VCO.



Blockdiagram RTR6250

5.3.2 GSM dual band TX VCO

• The GSM TX VCO (Z300) is external to the RTR6250 and uses filtered signals (GSM_TX_CP) from the RTR6250 to provide the GMSK signal to the power amplifier.

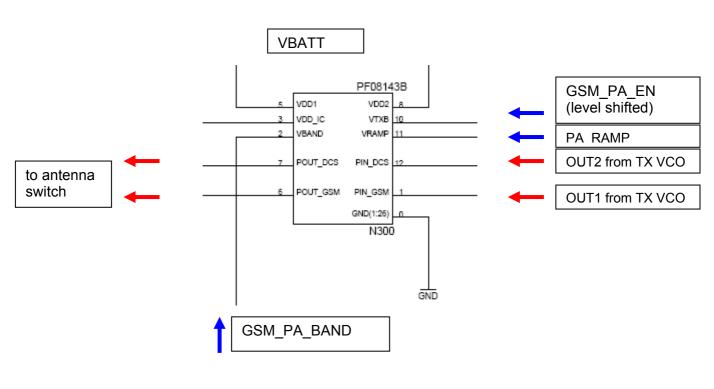


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5.3.3 GSM power amplifier

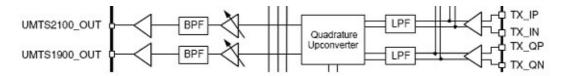
The output signals (OUT1 and OUT2) from the GSM TX VCO are led to the power amplifier. The power amplifier is the PA-module N300. It contains of two separate amplifier chains for GSM900 and GSM1800/GSM1900 operation. The amplification is controlled with the signal VRAMP. The appropriate amplifier chain is activated by the logic signal GSM_PA_BAND which is provided by the MSM6250. The N300 is activated through the signal VTXB, which is the level shifted GSM_PA_EN provided by the MSM6250. The voltage VBATT is provided by the battery.



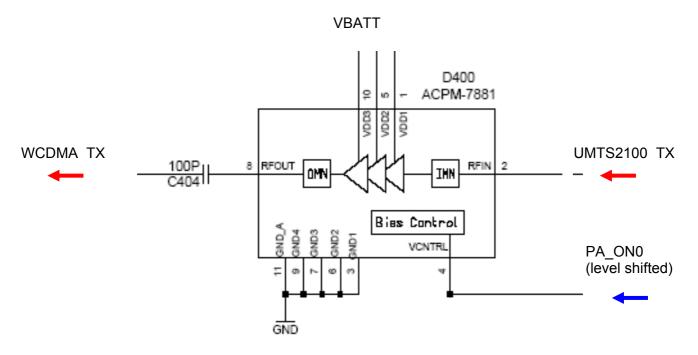
Circuit diagram (sheet 3)

5.3.4 UMTS TX

The IQ signals from the baseband are directly up-converted to the RF band by a Quadrature Upconverter and passed to the external filter. The UMTS 1900 TX path is not used in the SXG75.



Blockdiagram RTR6250



Circuit diagram (sheet 4)

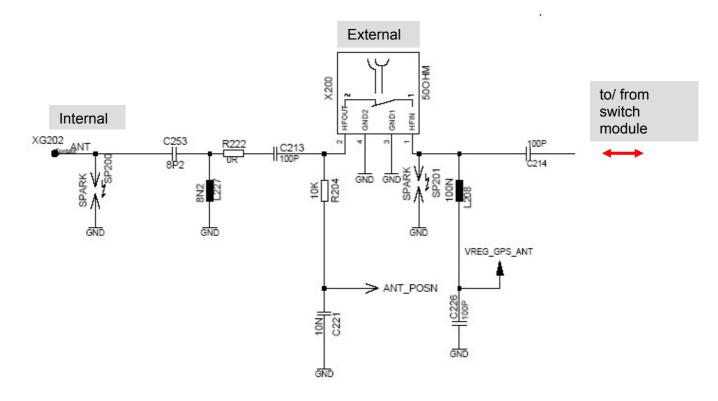
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5.4 Antenna switch

The SXG75 mobile has two antenna switches:

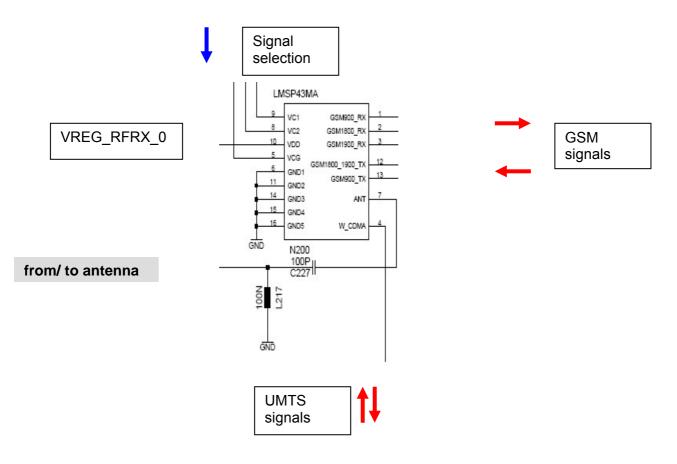
a) The mechanical antenna switch for the differentiation between the internal and external antenna.

Internal/external antenna switch



Circuit diagram (sheet 2)

Technical Documentation TD_Repair_L3_SXG75_R1.0.pdf 01/2006 Page 15 of 73 1) The electrical antenna switch for the differentiation between the GSM and UMTS receiving respectively transmitting signals.

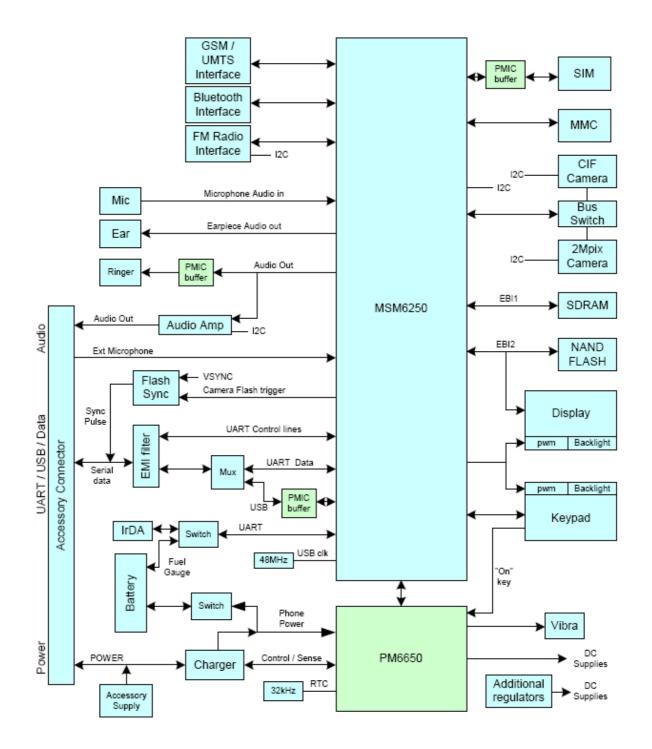


Circuit diagram (sheet 2)

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6 Baseband

6.1 Block diagram



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6.2 MSM6250 processor

6.2.1 General features

- Supports UMTS FDD release 99 September 2002 standard air interface
- Supports GSM/GPRS in addition to W-CDMA
- Supports low-power, low-frequency crystal to enable TCXO shutoff

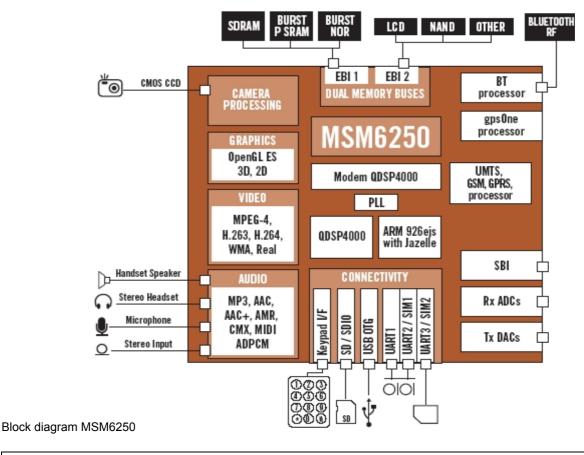
• radioOne™ Zero IF interface Zero IF support - DC offset cancellation and digital variable gain amplifier

Software-controlled power management features

• Hardware support for inter-frequency and inter-radio access technology searching in CM (WCDMA-GSM)

• Higher-speed serial bus interface, operating at up to 10 MHz and capable of handling four hardware requests

- Multimedia card hardware support
- Serial bus controller: standard 100 kbps and fast 400 kbps
- MPEG4 video encoder
- 2-D and 3-D graphics accelerator for gaming applications
- · Hardware acceleration supporting video capture and video telephony
- USB slave functionality
- Integrated wideband stereo CODEC for digital audio application



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6.2.2 MSM6250 power supplies

The supplies used by the MSM6250 are generated by the PM6650 (Section 5). They are as follows:

Supply Name	Value	Power Domain
VREG_MSMC	1.375 V (±3%)	Digital Core only.
VREG_MSME	1.850 V (±3%)	SDRAM interface (EBI1 bus), NAND FLASH and LCD interface (EBI2 bus), supply voltage for IO Pad group 2
VREG_MSMA	2.600 V (±3%)	Analog circuits
VREG_MSMP	2.600 V (±3%)	Supply voltage for IO pad group 3

MSM6250 power supplies

Each supply has a zero-ohm series resistor (R804, R805, R806, R808) before the MSM6250 decoupling capacitors. The supplies become active while the phone is in the reset state during "Phone On" operation (PON_RST_N from the PM6650 is low). They remain active until the phone is turned off.

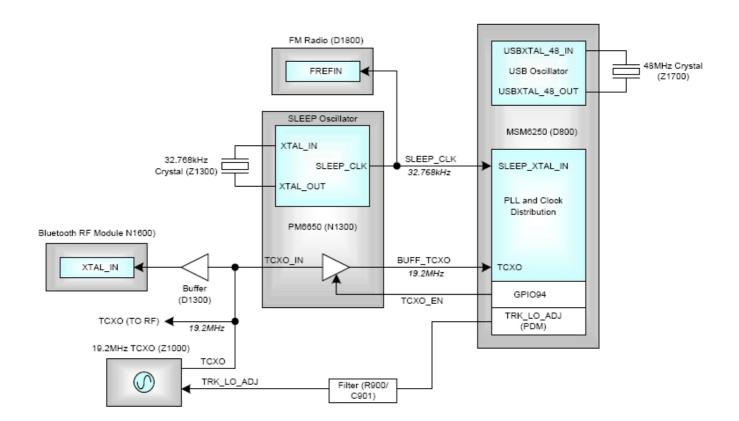
6.2.3 Clock distribution

The master clock for Wolf 5 baseband and RF systems runs at 19.2MHz. The clock is generated by Voltage-Controlled-Temperature-Compensated-Crystal-Oscillator Z1000. The clock is buffered to VREG_MSMP (2.6V) levels within the PM6650, and then sent to the MSM6250. The PM6650 buffer is enabled by logic control TCXO_EN from the MSM6250. The MSM6250 integrates a phase-locked loop and digital dividers to derive internal clocks from the TCXO clock input.

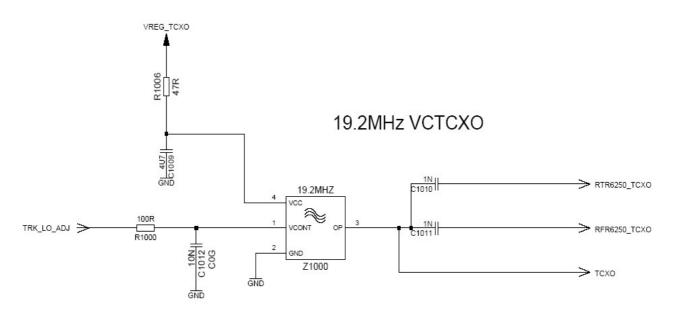
The TCXO is also buffered by D1300 to feed the Bluetooth RF Module, N1600. This buffer is only enabled when the Bluetooth supply (VREG_AUX2) is active.

A 32.768 kHz clock (SLEEP_CLK) is generated by the PM6650, and fed to the MSM6250. This clock is used for low-power operation during phone idle periods when the TCXO is disabled. It also drives a Real-Time-Clock circuit in the PM6650. The power supply for the Sleep Oscillator and associated Real-Time-Clock is derived from the battery voltage and backup capacitor C1312. This means the clock is active when the phone is powered off, and for 40 seconds when the battery is removed.

A 48MHz clock is provided by Z1700. This is used internally by the MSM6250 to control USB functions.



Block diagram



Circuit diagram (sheet 10)

The oscillator output signal *TCXO* is connected to the power management IC (PMIC, N1300, Pin 58).

The oscillator output signals *RFR6250_TCXO* and *RTR6250_TCXO* are connected to the RF chips RFR6250 (N600, Pin 33) resp. RTR6250 (D500, Pin 6).

To compensate frequency drifts the oscillator frequency is controlled by the *TRX_LO_ADJ* signal, generated through the MSM6250 (D800, SW_TP902).



Circuit diagram (sheet 9)

6.2.4 MSM6250 bootup and mode control

The MSM6250 supports booting from the NAND FLASH memory. The high pull-up (R1700) on the bootmode input pin is used to indicate to the MSM hardware that FLASH boot-up is required. After power-on reset, the MSM hardware automatically loads the boot code from NAND flash to an on-chip boot SRAM, and then releases the ARM to execute from this boot SRAM. By executing the boot code, the ARM processor transfers the entire phone software to the SDRAM, and then branches to the SDRAM to execute the phone software and completes the boot-up process. The MSM6250 runs in "Native" mode. This mode is selected by the Mode 0, Mode 1 and Mode 2

pins (Schematic sheet 17). The pins are left floating (internal pulldown resistors) to select Native mode. Note that the Mode pins are connected to additional MSM6250 pins. This is a requirement of the device – the signals are not required for any external functions.

MSM6250 Function	Signal	Function
ТСХО	BUFF_TCXO	TCXO clock input from PM6650
USB_XTAL48_IN	(48MHz crystal)	48 MHz crystal oscillator input
USB_XTAL48_OUT	(48MHz crystal)	48 MHz crystal oscillator
SLEEP_XTAL_IN	SLEEP_CLK	Low-power sleep crystal oscillator from PM6650
SLEEP_XTAL_OUT		(not used)
RESIN_N	PON_RST_N	Hardware reset input from PM6650
RESOUT_N		(not used)
RESOUT_N_EBI1	RESOUT1_N	Reset output generated by RESIN_N and by wdog_reset. Reset to LCD, NAND FLASH
WDOG_EN		(not used)
MODE[2]		(not used)
MODE[1]		(not used)
MODE[0]		(not used)
BOOT_MODE		pull-up to VREG_MSMP (boot from NAND)

MSM6250 clocks and mode control

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6.3 MSM6250 interfaces

6.3.1 Logic interfaces

Each IO pin on the MSM6250 has an associated pad group. The pad group, and hence the IO pin, is powered from the supplies as below:

Pad Group	Pad		Pad Group Connections	
1	VREG_MSME	1.850 V (±3%)	EBI1 bus to SDRAM	
2	VREG_MSME	1.850 V (±3%)	EBI2 bus to NAND FLASH and LCD. Plus some GPIO	
3	VREG_MSMP	2.600 V (±3%)	Most peripheral interfaces	
4	VREG_MSMP	2.600 V (±3%)	SIM bus (to PM6650). Plus one GPIO.	

MSM6250 pad group supplies

The maximum and minimum possible logic levels seen on the I/O pins (allowing for maximum supply variation and loading) should be within:

Pad Group	Vo∟ min (V)	Vo∟ max (V)	V _{OH} min (V)	V _{он} max (V)	V _{iL} min (V)	V _{iL} max (V)	V _{iH} min (V)	V _{iH} max (V)
1, 2	0	0.45	1.344	1.906	-0.3	0.628	1.239	2.085
2, 3	0	0.45	2.027	2.678	-0.3	0.883	1.741	2.822

MSM6250 logic specification

Peripheral systems on the phone are controlled by the MSM6250 logic signals listed below. These signals uses General Purpose IO (GPIO) pins on the MSM6250 and are configured to perform the required function by software.

A brief description of the signals is given in the following table:

Release	1	0
i tolouoo		

GPIO	Pad GP	Signal Name	Function
0	3	CAM1_PWR_EN	Mpix camera regulator enable. Active high.
1	3	CAM2_PWR_EN	CIF camera regulator enable. Active high
2	3		
3	3	PS_HOLD	PM6650. Held high to latch phone power ON.
4	3	GSM_PA_EN	RF system control.
5	3	GSM_PA_BAND	RF system control.
6	3	LOW_VOL	(Not used)
7	3	TX_VCO_1_EN_N	RF system control.
8	3	TX_VCO_0_EN_N	RF system control.
9	3	ANT_SEL0	RF system control.
10	3	ANT_SEL1	RF system control.
11	3	ANT_SEL2	RF system control.
12	3	BT_ENABLE	Bluetooth (Not used)
13	3	LCD_BCKLT_PWM	LCD and keypad backlight PWM signal for current control.
14	3	CAMIF_PCLK	Camera bus switch. Pixel clock.
15	3	CAMIF_HSYNC	Camera bus switch. Sync pulse.
16	3	CAMIF_VSYNC	Camera bus switch. Sync pulse.
17	3	ANT_POSN	External antenna sense.
18	3	A_RDS_DATA_EXIST	FM radio interrupt.
19	3	CAMIF_DSP_CLK	Camera bus switch. Master clock to cameras
20	3	BT_DATA	Bluetooth interface.
21	3	BT_TX_RX_N	Bluetooth interface.
22	3	BT_SBDT	Bluetooth interface.
23	3	BT_SBCK	Bluetooth interface.
24	3	BT_SBST	Bluetooth interface.
25	3	BT_CLK	Bluetooth interface.
26	3	I2C_SDA	I2C bus to cameras, FM radio and audio amplifier.
27	3	I2C_SCL	I2C bus to cameras, FM radio and audio amplifier.
28	3	LCD_EN	LCD Regulator enable. Active high.
29	3	A_FM_STANDBY	FM Radio enable.
30	3	MMC_CMD	MMC interface.
31	3	MMC_CLK	MMC interface.
32	3	MMC_DATA	MMC interface.
33	2	NAND_FLASH_READY	NAND FLASH interface.
34	2	A2(20)	LCD interface.
35	2	MMC_CD	MMC interface.
36	2	BACKLIGHT_EN	Backlight switcher supply enable. Active high.

37	2	ETM detect	Pull-down resistor used on ETM board version only.
38	2	LCD2_CS_N	LCD interface.
39	3	MSM_UART1_DCD_N	Accessory connector UART signal.
40	3	 PM_INT_N	PM6650 interrupt to MSM6250.
41	3	FUEL_GAUGE_1	(Not used)
42	3		(Not used. required for ETM board version only)
43	3		(Not used. required for ETM board version only)
44	3		(Not used. required for ETM board version only)
45	3	KYPD_MEMO	Keypad matrix driver.
46	3	KEYSENSE_N[2]	Keypad matrix sensor line.
47	3	KEYSENSE_N[3]	Keypad matrix sensor line.
48	3	KEYSENSE_N[4]	Keypad matrix sensor line.
49	3	KYPD_9	Keypad matrix driver.
50	3	KYPD_11	Keypad matrix driver.
51	3	KYPD_13	Keypad matrix driver.
52	3	KYPD_15	Keypad matrix driver.
53	3	KYPD_17	Keypad matrix driver.
54	3	CAMIF_DATA(0)	Camera bus switch. Data from camera.
55	3	CAMIF_DATA(1)	Camera bus switch. Data from camera.
56	3	CAMIF_DATA(2)	Camera bus switch. Data from camera.
57	3	CAMIF_DATA(3)	Camera bus switch. Data from camera.
58	3	CAMIF_DATA(4)	Camera bus switch. Data from camera.
59	3	CAMIF_DATA(5)	Camera bus switch. Data from camera.
60	3	CAMIF_DATA(6)	Camera bus switch. Data from camera.
61	3	CAMIF_DATA(7)	Camera bus switch. Data from camera.
62	3	KEYSENSE_N(0)	Keypad matrix sensor line.
63	3	KEYSENSE_N(1)	Keypad matrix sensor line.
64	3		(Not Used. required for ETM board version only)
65	3		(Not Used. required for ETM board version only)
66	3		(Not Used. required for ETM board version only)
67	1	SDRAM1_D(16)	SDRAM interface.
68	1	SDRAM1_D(17)	SDRAM interface.
69	1	SDRAM1_D(18)	SDRAM interface.
70	1	SDRAM1_D(19)	SDRAM interface.
71	1	SDRAM1_D(20)	SDRAM interface.
72	1	SDRAM1_D(21)	SDRAM interface.
73	1	SDRAM1_D(22)	SDRAM interface.
74	1	SDRAM1_D(23)	SDRAM interface.
75	1	SDRAM1_DQM(3)	SDRAM interface.
76	1	(KYPD_INT_N)	(Not Used. required for ETM board version only)
77	1	LCD_VSYNC	LCD interface.
78	1	SDRAM1_DQM(2)	SDRAM interface.

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79	1	SDRAM_A1(0)	SDRAM interface.		
80	3	PM SBCK	PM6650 serial port. MSM <> PM6650 communication.		
81	3	PM SBST	PM6650 serial port. MSM <> PM6650 communication.		
82	3	PM SBDT	PM6650 serial port. MSM <> PM6650 communication.		
83	3	USB_RS232_SEL1	USB / UART select control. High for UART selection.		
84	3	IRDA_TXD	IrDA interface.		
85	3	IRDA_RXD	IrDA interface.		
86	3	ACC_PWR_EN	Accessory power supply enable. Active high.		
87	3	FLASH_EN	Accessory connector. Clip-on camera flash enable.		
88	4	USIM_DATA	SIM interface (PM6650 Buffer)		
89	4	CAM1_SEL_N	Camera bus switch. Enable for Mpix camera. Active low.		
90	4	USIM_RST	SIM interface (PM6650 Buffer)		
91	4	USIM_CLK	SIM interface (PM6650 Buffer)		
92	3	HPH_SD	(Not used)		
93	3	CAM2_SEL_N	Camera bus switch. Enable for CIF camera. Active low.		
94	3	TCXO_EN	PM6650 interface. Enable for TCXO Controller.		
95	3	MSM_UART1_TXD	Accessory connector. Serial data out.		
96	3	MSM_UART1_RXD	Accessory connector. Serial data in.		
97	3	MSM_UART1_CTS_N	Accessory connector UART signal.		
98	3				

MSM6250 GPIO functions

The MSM6250 has additional dedicated lines for interfaces to the SDRAM, NAND FLASH, RF system and USB functions.

Communication with the other major components of the Qualcomm chipset uses the following synchronous serial ports:

Serial Bus	Connects to
SBST_0, SBDT_0,	
SBCK_0	RF System. RTR6250, RFR6250
PM_SBST, PM_SBDT,	
PM_SBCK	Power Management. PM6650
BT_SBST, BT_SBDT,	
BT_SBCK	Bluetooth. BCM2004

MSM6250 communication ports

6.3.2 Analogue interfaces

The analogue functions in the MSM6250 are powered from the VREG_MSMA (2.6V) supply.

Signal functions are summarised below:

MSM6250 Function	Signal Name	Function		
MIC1P	MIC1_P	Mic 1 input (+) to phone microphone		
MIC1N	MIC1_M	Mic 1 input (-) to phone microphone		
MIC2P	MIC2_P	Mic 2 input (+) to accessory connector mic input		
MIC2N	MIC2_M	Mic 2 input (-) to accessory connector mic input		
AUXIP_AUXIL	FM_RADIO_AUXI P	FM radio input (left)		
AUXIN_AUXIR	FM_RADIO_AUXI P	FM radio input (right)		
EAR10P	EAR10_P	Earphone 1 amplifier output (+) to earpiece		
EAR10N	EAR10_M	Earphone 1 amplifier output (-) to earpiece		
HPH_L		Not used		
HPH_R		Not used		
AUXOP_AUXO L AUXO_P		Auxiliary output (+/Left) to PM6650 amplifier, and accessory amplifier.		
AUXON_AUXO R	AUX_M	Auxiliary output (-/Right) to PM6650 amplifier, and accessory amplifier.		
HKIN[5]		ADC analogue input. Hardware identification on A1+ and above		
HKIN[4]		ADC analogue input. Hardware identification on A1+ and above		
HKIN[3]	PA_THERM	ADC analogue input. From PA temperature sensor.		
HKIN[2]	HDET1	ADC analogue input. From RF power level sensor.		
HKIN[1]	RF_THERM	ADC analogue input. From second temperature sensor. Not used on version B2.2 and above.		
HKIN[0]	AMUX_OUT	ADC analogue input. From PM6650 analogueue signal input (battery voltage etc)		
I_IP_CH1	RX1_I_P			
I_IM_CH1	RX1_I_M	From analogue IQ output from GPS receiver (RFR6250)		
Q_IP_CH1	RX1_Q_P			
Q_IM_CH1	RX1_Q_M			
I_IP_CH0	RX0_I_P	From analogue IQ output from UMTS receiver (RFR625		

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I_IM_CH0	RX0_I_M	and from analogue IQ output from GSM receiver	
Q_IP_CH0	RX0_Q_P	(RTR6250)	
Q_IM_CH0	RX0_Q_M		
I_OUT	TX_I_P		
I_OUT_N	TX_I_M	To analogue IQ inputs of the RF transceiver (RTR6250)	
Q_OUT	TX_Q_P		
Q_OUT_N	TX_Q_M		

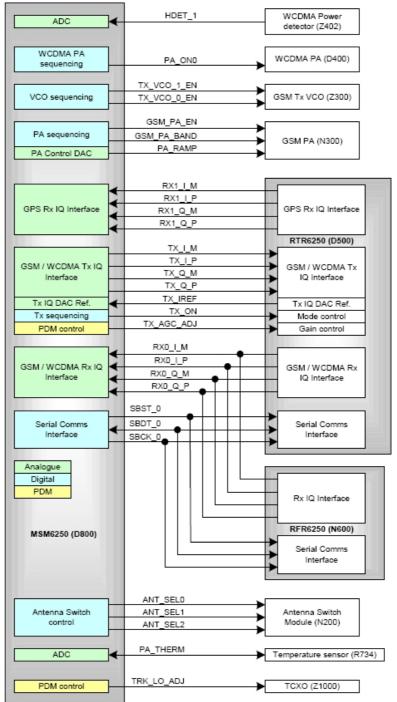
MSM6250 analogue interfaces

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6.3.3 RF interfaces

The MSM6250 provides the baseband controls for the RF section of the phone. Control and signal interfaces are shown below.



Signal	Function			
WCDMA Power Detector				
HDET1	Voltage proportional to TX power of WCDMA signal. Fed to HKAIN2 input to MSM6250 ADC multiplexer.			
WCDMA PA				
PA_ON0	Logic control to enable PA Turns the PA on and off as required to support UMTS operation while consuming minimum DC current.			
GSM Tx VCO				
TX_VCO_1_EN_N	Logic control to set VCO operating band. TX_VCO_0_EN_N = 0, TX_VCO_1_EN_N =1 > high band			
TX_VCO_0_EN_N	TX_VCO_0_EN_N =1, TX_VCO_1_EN_N =0 > low band			
GSM PA				
GSM_PA_EN	Logic control to enable GSM PA. Steps the PA gain and bias, greatly reducing DC current consumption under typical operating conditions.			
GSM_PA_BAND	Logic control to set GSM PA operating band.			
GSM_PA_RAMP	DAC voltage to set GSM PA power. A control line that is filtered within the automatic power control circuits to smoothly ramp the PA on prior to transmit energy being applied.			
RTR6250 GPS Rx IQ Interfa	ce			
RX1_I_M				
RX1_I_P	Received GPS IQ signals. The IQ signals are concerted to digital by			
RX1_Q_M	analog-to-digital converter (ADC) circuit within the MSM6250 IC.			
RX1_Q_P	-			
RTR6250 GSM / WCDMA T	x IQ Interface			
TX_I_M	Transmit IQ signals. The transmit baseband signals are generated by digital-to-analog converter (DAC) circuit within the MSM6250 IC.			
TX_I_P	Transmit CDC IO signals. The IO signals are concerted to divited by			
TX_Q_M	Transmit GPS IQ signals. The IQ signals are concerted to digital by analog-to-digital converter (ADC) circuit within the MSM6250 IC.			
TX_Q_P				
TX_IREF	DAC reference voltage provided by the RTR6250. Used to improve TX IQ DAC signal quality.			
RTR6250 Tx system controls				
TX_ON	Logic control. Used to control the RTR6250 operating mode.			
TX_AGC_ADJ	A pulse-density modulated digital signal from the MSM6250. It is filtered by R902/C900 to form an analogue control voltage. This voltage is used to set the WCDMA transmitter power.			

RTR6250 GSM / WCDMA Rx IQ Interface			
RX0_I_M			
RX0_I_P	Received GSM and WCDMA IQ signals. The IQ signals are concerted to digital by analog-to-digital converter (ADC) circuits within the MSM6250 IC.		
RX0_Q_M			
RX0_Q_P			
RTR6250 / RFR6250 Serial	Comms Interface		
SBST_0	The RTR6250 and RFR6250 operating modes and circuit parameters are MSM-controlled through the proprietary 3-line serial bus interface.		
	The serial bus strobe signal is used by the MSM6250 to initiate serial data transfers.		
SBDT_0	The serial bus data line is a bi-directional data line that transfers data into and out of the ICs. All ICs configure this line as a tri-state driver for output functions and as a CMOS gate for input functions. No external pull-up resistor is needed.		
SBCK_0	The serial bus clock synchronizes data transfers.		
Antenna Switch Module Inter	face		
ANT_SEL0	Logic controls. ANT_SEL0=0, ANT_SEL1=0, ANT_SEL2=1 >		
ANT_SEL1	GSM900TX, ANT_SEL0=0, ANT_SEL1=0, ANT_SEL2=0 > GSM900RX/WCDMA, ANT_SEL0=1, ANT_SEL1=1, ANT_SEL2=0 > GSM1800/1900TX.		
	ANT SEL0=0, ANT SEL1=1, ANT SEL2=0 > GSM1800RX.		
	ANT_SEL0=1, ANT_SEL1=0, ANT_SEL2=0 > GSM1900RX.		
ANT_SEL2			
Antenna Position Sensor			
ANT_POSN	Logic signal to MSM6250. This line is pulled high when an external antenna is fitted.		
PA temperature sensor			
PA_THERM	Voltage proportional to PA temperature from thermistor circuit (R734/R732). Fed to HKAIN3 input to MSM6250 ADC multiplexer.		
TCXO control			
TRK_LO_ADJ	A pulse-density modulated digital signal from the MSM6250. It is filtered by R900/C901 to form an analogue control voltage. The analogue voltage is used to adjust the operating frequency of the TCXO.		

RF interface signals

7 FM Radio

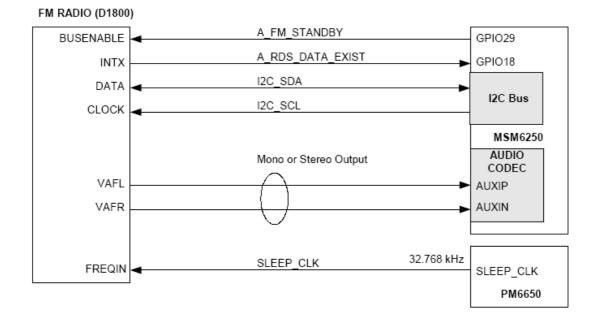
The output from the Philips FM radio chip is fed into the auxiliary input of the MSM6250 audio CODEC.

This is the routed directly to the auxiliary outputs of the MSM6250 via a built in gain stage. FM radio can be played in stereo or mono mode, depending upon signal quality and/or user selection. FM radio can only be played back with a stereo headset or mobile sound set connected to the accessory connector.

This is because these are the only accessories that contain an effective FM antenna, which is implemented using an antenna connected to MIC_GND.

In addition, the output of the FM radio can be routed to the hands-free speaker. A stereo headset is still required to provide the antenna.

7.1 FM radio interface



The analogue sections of the radio are powered from VREG_MSMA (2.6V). The digital interfaces are powered from VREG_MSMP (2.6V).

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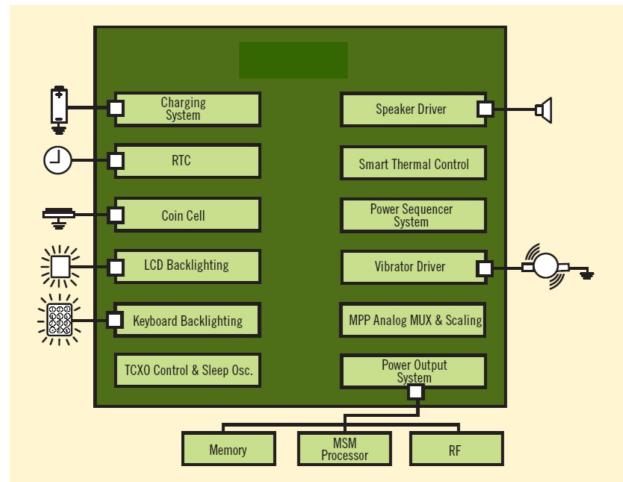
Interface signals are:

Signal	Function			
SLEEP_CLK	32.768MHz clock from PM6650. Used as master clock for FM system.			
	Logic output from FM radio.			
A_RDS_DATA_EXIST	Provides an interrupt signal to MSM6250. The radio takes this line low for 10ms to indicate that it has new RDS data, or that some other action is required by the MSM6250.			
I2C_SDA	I2C data to configure the radio and to transfer RDS data. I2C address is 0010000 (FM radio part), and 0010001 (RDS part).			
I2C_SCL	I2C clock.			
	Logic input from MSM6250.			
A_FM_STANDBY	This disables the I2C interface when held low. This is required (in addition to configuring internal registers) to put the device into a minimum-current Standby mode.			
FM_RADIO_AUXIP	Audio out (left channel). Fed to AUXIP audio input on MSM6250.			
FM_RADIO_AUXIN	Audio out (right channel). Fed to AUXIN audio input on MSM6250.			

FM radio interface signals

8 Power management

8.1 PM6650 functional overview



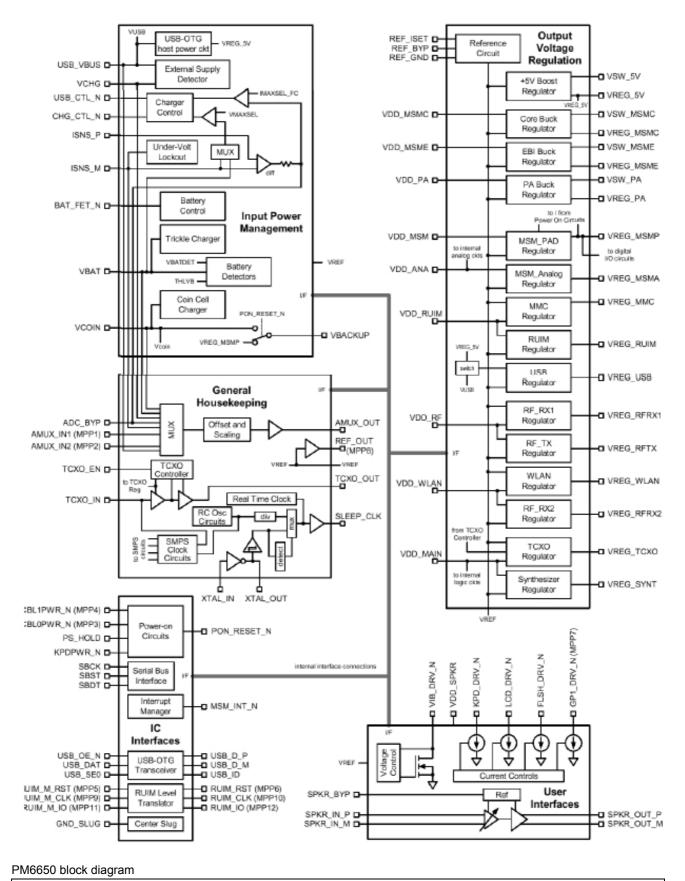
PM6650 functions

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8.2 Voltage regulators and voltage converters

The table below lists the voltage supplies of the PM6650. Note that the rated current is the current at which the regulator meets all its performance specifications. Higher currents are allowed but higher input voltages may be required and some performance characteristics may become degraded.

PM6650 Supply Source	Supply Net Name	Voltage range	Voltage set to	Baseband Supplies	RF Supplies
VREG_RFRX_ 1	VREG_RFRX_ 0	1.50 -3.05V (150mA)	2.85V		N200 (Antenna switch), D500 (RTR6250), RF3188 WCDMA PA.
VREG_RFRX_ 2	VREG_RFRX_ 1	1.50 -3.05V (150mA)	2.85V		N600 (RFR6250)
VREG_RFTX	VREG_RFTX	1.50 -3.05V (150mA)	2.85V		Z402 (power detector), D500 (RTR6250), Z300 (GSM VCO)
VREG_PA (Step-down Switcher)	(not used)	0.75 -3.05V (500mA)	Vari- able		Not used
VREG_SYNT	VREG_SYNTH	1.50 -3.05V (50mA)	2.85V		D500 (RTR6250),
VREG_TCXO	VREG_TCXO	1.50 -3.05V (50mA)	2.85V	D1300 (Bluetooth clock buffer),	Z1000 (TCXO), N600 (RFR6250),
VREG_MSMP	VREG_MSMP	1.50 -3.05V (300mA)	2.6V	V2100 (IrDA), N1600 (Bluetooth IC), D1900/1901 (Camera Bus Switch), D800 (MSM6250 VDD_P3, VDD_P4), Z1200 (EMIF05MUX)	N600 (RFR6250), D500 (RTR6250), D1800 (FM Radio),

VREG_MSME (Step-down Switcher)	VREG_MSME	0.75 -3.05V (500mA)	1.85V	X2201 (LCD), D1000 (NAND FLASH), D1001 (SDRAM), D800 (MSM6250 VDD_P2, VDD_P1)	
VREG_MSMC (Step-down Switcher)	VREG_MSMC	0.75 -3.05V (500mA)	1.375V	D800 (MSM6250 VDD_C)	
VREG_MSMA	VREG_MSMA	1.50 -3.05V (300mA)	2.6V	D800 (MSM6250 VDD_A), D800 (MSM6250 VDD_PLL), D800 (MSM6250 VDD_DAC), N700 (Audio Amp), Hardware ID,	D1800 (FM Radio), RF/PA temperature sense,
VREG_MMC	VREG_AUX1	1.50 -3.05V (150mA)	2.85V	X1400 (MMC Card)	
VREG_WLAN	VREG_AUX2	1.50 -3.05V (150mA)	2.85V	N1600 (Bluetooth IC)	
VREG_RUIM	VREG_UIM	1.50 -3.05V (150mA)	3.0v	Z1500 (SIM Card)	
VREG_5V (Step-up Switcher)	(Used internally to PM6650 for USB)	3.0 - 6.1V (400mA)	5V		Used for gen- eration of VREG_USB
VREG_USB	(not used)	3.30V (50mA)	3.3V		On board USB functions

PM6650 power supplies

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8.3 Additional power supplies

The following additional external regulators are required:

Regula- tor	Supply Net Name	Voltage set to	Supplies	Enabled by
N1900	VREG_CAM1 (2)	2.85V / 2.85V	Camera 1 and 2	CAM1_PWR_EN CAM2_PWR_EN
N2201	(none) Supply on the LCD connector	2.9V	LCD (on EBI2 bus)	LCD_EN
N1100	POWER (for external supply)	3.48V @300mA	Accessory Connec- tor	ACC_PWR_EN
N900	VREG_BCKLT LCD and Keypad Backlight for A1+	18.75V	LCD and Keypad Backlight on A1+. Not used on A1.	BACKLIGHT_EN

PM6650 additional regulators

8.4 PM6650 signal interfaces

The PM6650 contains many additional functions as well as power supply regulators. The main signal interfaces to these functions are summarised here.

PM6650 Function	Signal	Function		
Clock interfaces	6.			
	is buffered to VREG_MSM gulator are enabled by the	IP and fed to the MSM6250. The buffer and MSM6250.		
The 32.768kHz S	Sleep clock is generated or	the PM6650 and fed to the MSM6250 and FM radio.		
TCXO_EN	TCXO_EN	Control input from MSM6250 to enable TCXO tasks		
TCXO_IN	ТСХО	19.2MHz signal input		
TCXO_OUT	BUFF_TCXO	Buffered 19.2MHz signal fed to MSM6250		
SLEEP_CLK	SLEEP_CLK	32.768 kHz sleep clock signal. Fed to MSM sleep clock Input, and FM radio clock input.		
SIM Card interfaces.				
The SIM signals to/from the MSM6250 are level-shifted to VREG_UIM levels.				
RUIM_M_RST	USIM_RESET	SIM signal level shifter interface to MSM6250		
RUIM_RST	UIM_P_RESET	SIM signal level shifter interface to SIM Card		
RUIM_M_CLK	CLK USIM_CLK SIM signal level shifter interface to MSM6250			
RUIM_CLK	UIM_P_CLK	SIM signal level shifter interface to SIM Card		

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RUIM_M_IO	USIM_DATA	SIM signal level shifter interface to MSM6250
RUIM_IO	UIM_P_DATA	SIM signal level shifter interface to SIM Card
USB Interface.		
The MSM6250	USB signals interface to	a USB transceiver on the PM6650
USB_OE	USB_OE_TP_N	USB interface to MSM6250
USB_DAT	USB_DAT_VP	USB interface to MSM6250
USB_SE0	USB_SE0_VM	USB interface to MSM6250
USB_D_P	USN_CONN_D_P	USB interface to connector via UART/USB switch
USB_D_M	USB_CONN_D_M	USB interface to connector via UART/USB switch
/USB_CTL	(no connection)	(not used)
USB_ID	(no connection)	(not used)
USB_VBUS	(47K to ground)	(not used)
Charger Funct	ions.	
	enses the charger and ba	ttery voltages, and charge current, to control the charging
process.	DOW/FR	
VCHG	POWER	Charger voltage sense line for charging functions
ISNS_M	ICHARGEOUT	Charging current sense input
ISNS_P	ICHARGE	Charging current sense input
CHG_CTL	CHG_CNT_N	Charger transistor control
Vbat	VBATT	Battery voltage sense line for charging functions
Vbat BAT_FET_N	VBATT	Battery voltage sense line for charging functions
Vbat BAT_FET_N Audio Buffer.	VBATT BAT_FET	Battery voltage sense line for charging functions Battery MOSFET control
Vbat BAT_FET_N Audio Buffer. The Audio outp	VBATT BAT_FET ut from the MSM6250 is a	Battery voltage sense line for charging functions Battery MOSFET control amplified to drive the ringer speaker.
Vbat BAT_FET_N Audio Buffer. The Audio outp SPKR_IN_M	VBATT BAT_FET ut from the MSM6250 is a AUXO_M	Battery voltage sense line for charging functions Battery MOSFET control amplified to drive the ringer speaker. Speaker Drive Amp input
Vbat BAT_FET_N Audio Buffer. The Audio outp SPKR_IN_M SPKR_IN_P	VBATT BAT_FET ut from the MSM6250 is a	Battery voltage sense line for charging functions Battery MOSFET control amplified to drive the ringer speaker.
Vbat BAT_FET_N Audio Buffer. The Audio outp SPKR_IN_M	VBATT BAT_FET ut from the MSM6250 is a AUXO_M	Battery voltage sense line for charging functions Battery MOSFET control amplified to drive the ringer speaker. Speaker Drive Amp input
Vbat BAT_FET_N Audio Buffer. The Audio outp SPKR_IN_M SPKR_IN_P SPKR_OUT_	VBATT BAT_FET ut from the MSM6250 is a AUXO_M AUXO_P	Battery voltage sense line for charging functions Battery MOSFET control amplified to drive the ringer speaker. Speaker Drive Amp input Speaker Drive Amp input
Vbat BAT_FET_N Audio Buffer. The Audio outp SPKR_IN_M SPKR_IN_P SPKR_OUT_ M	VBATT BAT_FET ut from the MSM6250 is a AUXO_M AUXO_P SPKR_OUT_M SPKR_OUT_P	Battery voltage sense line for charging functions Battery MOSFET control amplified to drive the ringer speaker. Speaker Drive Amp input Speaker Drive Amp input Speaker Drive Amp output
Vbat BAT_FET_N Audio Buffer. The Audio outp SPKR_IN_M SPKR_IN_P SPKR_OUT_ M SPKR_OUT_P MSM6250 Com	VBATT BAT_FET ut from the MSM6250 is a AUXO_M AUXO_P SPKR_OUT_M SPKR_OUT_P	Battery voltage sense line for charging functions Battery MOSFET control amplified to drive the ringer speaker. Speaker Drive Amp input Speaker Drive Amp input Speaker Drive Amp output
Vbat BAT_FET_N Audio Buffer. The Audio outp SPKR_IN_M SPKR_IN_P SPKR_OUT_ M SPKR_OUT_P MSM6250 Com	VBATT BAT_FET ut from the MSM6250 is a AUXO_M AUXO_P SPKR_OUT_M SPKR_OUT_P munication.	Battery voltage sense line for charging functions Battery MOSFET control amplified to drive the ringer speaker. Speaker Drive Amp input Speaker Drive Amp input Speaker Drive Amp output
Vbat BAT_FET_N Audio Buffer. The Audio outp SPKR_IN_M SPKR_IN_P SPKR_OUT_ M SPKR_OUT_P MSM6250 Corr Uses a synchro	VBATT BAT_FET ut from the MSM6250 is a AUXO_M AUXO_P SPKR_OUT_M SPKR_OUT_P munication.	Battery voltage sense line for charging functions Battery MOSFET control amplified to drive the ringer speaker. Speaker Drive Amp input Speaker Drive Amp input Speaker Drive Amp output Speaker Drive Amp output
Vbat BAT_FET_N Audio Buffer. The Audio outp SPKR_IN_M SPKR_IN_P SPKR_OUT_ M SPKR_OUT_P MSM6250 Com Uses a synchro SBDT	VBATT BAT_FET ut from the MSM6250 is a AUXO_M AUXO_P SPKR_OUT_M SPKR_OUT_P munication. mous serial interface. PM_SBDT	Battery voltage sense line for charging functions Battery MOSFET control amplified to drive the ringer speaker. Speaker Drive Amp input Speaker Drive Amp input Speaker Drive Amp output
Vbat BAT_FET_N Audio Buffer. The Audio outp SPKR_IN_M SPKR_IN_P SPKR_OUT_ M SPKR_OUT_P MSM6250 Com Uses a synchro SBDT SBCK	VBATT BAT_FET ut from the MSM6250 is a AUXO_M AUXO_P SPKR_OUT_M SPKR_OUT_P munication. mous serial interface. PM_SBDT PM_SBCK	Battery voltage sense line for charging functions Battery MOSFET control amplified to drive the ringer speaker. Speaker Drive Amp input Speaker Drive Amp input Speaker Drive Amp output
Vbat BAT_FET_N Audio Buffer. The Audio outp SPKR_IN_M SPKR_IN_P SPKR_OUT_ M SPKR_OUT_P MSM6250 Com Uses a synchro SBDT SBCK SBST	VBATT BAT_FET ut from the MSM6250 is a AUXO_M AUXO_P SPKR_OUT_M SPKR_OUT_P munication. nous serial interface. PM_SBDT PM_SBCK PM_SBST	Battery voltage sense line for charging functions Battery MOSFET control amplified to drive the ringer speaker. Speaker Drive Amp input Speaker Drive Amp input Speaker Drive Amp output
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Release 1.0

AMUX_IN2	LCD_RST_N	LCD Reset.			
Current control	Current control.				
The vibramotor is	s driven by a current sink fo	unction on the PM6650			
/VIB_DRV	VIB_DRV	Current sink for Vibrator Motor			
Power Manager	nent.				
Power on/off and	l backup functions				
VCOIN	(100uF capacitor, C1312)	Back-up capacitor. 100uF for 40 sec backup			
/PON_RST	PON_RST_N	Reset output to MSM6250			
/KPDPWR	PHONE_ON	Direct connection to Power / End key			
PS_HOLD	PS_HOLD / JTAG_PS_HOLD	Power latch from MSM / JTAG			
Analogue Multiplexer.					
Analogue voltages sensed on the PM6650 are fed to an ADC on the MSM6250 for measurement.					
AMUX_OUT	AMUX_OUT	Multiplexer output to MSM6250 ADC			

PM6650 signal interfaces

8.5 Power On/Off sequencing

8.5.1 Power-On sequence

The PM6650 includes circuitry to manage the power-on and off operations. Dedicated circuits continuously monitor events that might trigger a power-on sequence. If any of the events occurs, these circuits power-on the PM6650 IC and take the MSM device out of reset.

The inputs to the power-on circuit are:

• PHONE_ON. This is the input from the END/power key on the keypad. A low voltage on this line initiates the power-up sequence.

• Voltage detected on POWER line. This indicates that an external supply has been connected.

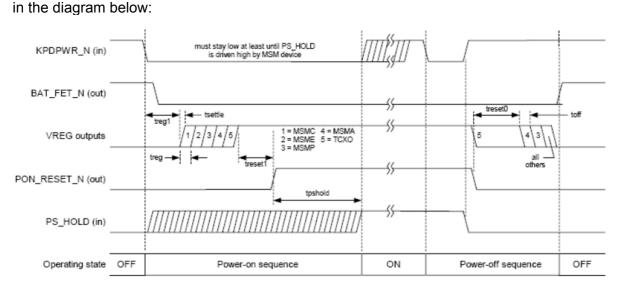
• Real Time Clock alarm triggered. While the PM6650 IC is off the Real Time Clock (RTC) and its oscillator source are still active. This allows continued monitoring of RTC alarms programmed via software. If an alarm occurs while the PM6650 IC is off an alarm interrupt is generated and the power-on sequence is initiated.

• Sudden Momentary Power Loss (SMPL) condition was detected and an SMPL recovery is initiated. If the power-on circuits detect that the SMPL function is enabled when the PS_HOLD signal is cleared, the power-on sequence is initiated.

The normal power-on sequence begins when the keypad power button is pressed; this pulls the PM6650 PHONE_ON input to the PM6650 low. At this point the PM6650 holds the reset output to the MSM6250 (PON_RST_N) low, and turns on the following power supplies in the following sequence:

- VREG_MSMC
- VREG_MSME
- VREG_MSMP
- VREG_MSMA
- VREG_TCXO

Technical Documentation TD_Repair_L3_SXG75_R1.0.pdf 01/2006 Page 40 of 73 As each regulator is enabled, detector circuits confirm that it powers up properly before triggering a wait interval. After the wait interval expires, the next regulator is enabled. This process continues until all the default-on regulators have powered up successfully. Once all the default-on regulators are on another wait interval is observed before the PON_RESET_N signal is driven high. For a successful power-on sequence, the MSM6250 must then initialise and drive the PS_HOLD signal high within a given time. If it does so, the power remains latched on. This sequence is shown



Power supply On/Off sequencing

8.5.2 Power-Off Sequence

The PM6650 is in an ON state while the PS_HOLD signal from the MSM6250 is high. Under this condition, the PM6650 continually monitors events that could trigger a power-off sequence:

• The MSM drives the PS_HOLD signal low in response to the handset user pressing the keypad power button.

• The PM6650 die temperature exceeds the over-temperature threshold.

The most common power-off sequence begins with the keypad power button being pressed while the MSM6250 is powered on and operational. The PM6650 PHONE_ON signal is connected to the handset keypad power button and is pulled up internally. The MSM6250 monitors the state of the key through interrupts from the PM6650. When an interrupt is triggered it initiates the following power-down sequence:

• The user presses and holds the END key for at least the minimum interval. The power-down sequence is aborted if not pressed long enough.

• Any information that needs to be saved is written to Flash ROM.

• The PM6650 is prevented from powering up again.

• The power-off sequence waits until the user releases the END key, otherwise the PM6650 IC will power-up again.

• The MSM6250 drives the PS_HOLD signal low to cause the PM6650 IC to power-down the handset.

• The PM6650 IC drives PON_RESET_N low to reset the MSM and other external devices, and disables the TCXO regulator. The PM6650 VBACKUP pin is internally connected to its VCOIN pin to provide backup power to SRAM.

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• After an interval several conditions are checked to determine the next action:

o If the over-temperature threshold was exceeded then the PON_RESET_N signal is immediately driven low and all PM6650 circuits are turned off. The over-temperature feature protects the PM6650 IC and cannot be disabled.

o If VPH_PWR is below the set threshold then the PON_RESET_N signal is immediately driven low and all PM6650 circuits are turned off. This feature protects the battery and cannot be disabled.

o If the over-temperature threshold was not exceeded, VPH_PWR is above the threshold, and the watchdog restart bit is set then the watchdog interrupt status bit is set, the MSM device is restarted, its watchdog timer is reset, and the PM6650 IC is restarted without fully powering down.

o If the over-temperature threshold was not exceeded, VPH_PWR is above the threshold, and the Sudden Momentary Power Loss (SMPL) function is enabled then the SMPL recovery is executed.

• If none of the above combinations occur, the normal power-down sequence is continued.

• The remaining regulators are powered down in the following sequence:

o VREG_MSMA o VREG_MSMP o all others

• An interval is allowed for both the MSMA and MSMP regulator outputs to discharge before all the other regulators are turned off. Another interval passes then the bandgap reference and all other unneeded circuits are disabled.

• The PM6650 IC turns off the battery MOSFET by driving BAT_FET_N high and makes sure the external supply is disconnected by driving CHG_CTL_N high. With all sources disconnected the PM6650 has no applied power and the phone is powered down.

• PM6650 IC is now OFF.

9 Battery/Charging

9.1 Battery

The battery is a high capacity Lilon - battery pack nominally rated at 4.2 V open circuit terminal voltage and about 1000 mAh minimal capacity. The battery pack has in-built electrical protection circuitry and contains a BQ27000 fuel gauge monitor from Texas Instruments. The fuel gauge signal is a 1-wire HDQ interface. See Section 13 for details of the fuel gauge interface. The battery pack has the following parameters:

The BQ27000 is programmed with the following parameters.

(Note: These parameters are subject to change, consequently if critical to work being undertaken it will be advisable to check these values)

- Initial LMD 914 mAh
- EDVF Threshold 3384 mV
- EDVI threshold 3592 mV
- Initial standby load 4.28 mA
- Digital filter threshold 4.9 μV
- Self discharge rate 0.11 % per day
- Taper current 76 mA
- Pack configuration 60 hex
- Initial max load 274.2 mA
- Dsg rate comp gain 9.8 %LMD/C-rate
- Dsg rate comp threshold 2 mAh Code (0~3)
- Temperature comp gain 1.46 %LMD/ °C
- Temp comp offset 14 °C

9.2 Phone shutdown due to low battery

Shutdown of the handset takes place in two stages. Both stages of shutdown are controlled in software depending on parameters read from the battery fuel gauge. The stages are:

• Stage 1: This occurs either when the fuel gauge reports 3.400V if the fuel gauge is reporting that it is uncalibrated, or when the fuel gauge reports that the first capacity limit has been passed by setting the EDV1 flag to 1.

• Stage 2: This occurs when the battery fuel gauge reports that the cell voltage has fallen below 3.200V. (Note that the fuel gauge EDVF flag is not used in current software)

Fuel gauge readings cannot be synchronised with GSM RF bursts so to avoid fluctuations in readings, the fuel gauge effectively applies a RC filter with a cut off frequency of 159Hz (time constant 6.3ms) to the readings to generate a filtered value which is reported via the digital interface.

The fuel gauge reports cell voltage not battery terminal voltage. Hence under high load conditions an error will exist if the cell voltage is assumed to be the handset battery terminal voltage or particularly the GSM PA voltage. The difference is greatest under high current supply conditions and worst case is full power

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01/2006 Page 43 of 73 GSM in which the RF PA current approaches 2A for full power transmit. Under these conditions the total voltage drop from cell to PA is in the order of 250mV.

With a calibrated cell at 25C the primary shutdown point is intended to occur when sufficient capacity remains to allow a 3 minute call at high power which is deemed to be a supply current of 350mA. The requirement is for 1 minute, hence 3 minutes is intended to allow some margin for cell aging and other effects.

9.3 Charging

All the important functions for the power supply of the phone are carried out by the PM6650 power management IC from Qualcomm. The POWER-pin of the I/O-Connector is for charging the battery with an external power supply.

The following restrictions must be observed:

• The phone cannot be operated without battery inserted.

• The phone will be damaged if the battery is inserted with wrong polarity (the mechanics of the phone prevent the battery from being put in the wrong way round. The electric system assumes that the battery has been inserted correctly. This must be ensured via suitable QA measures).

• It is inadvisable to remove the battery whilst the phone is connected to the charger unit however this action would not be expected to damage the phone.

If starting with a deeply discharge battery, charging must take place in three distinct phases. It is important during charging that the maximum battery terminal voltage does not exceed 4,2 V \pm 50 mV.

Trickle charging with a current below 100mA is only necessary when the battery voltage is less than 3.0 V.

The trickle charge current is set to 80mA.

The second phase is termed fast or constant current charging. The current for standard fast charging can be 950 mA max which is set by the maximum capability of the charger unit. The current limit of the PM6650 is set to 1.2A to ensure that the charger voltage folds back thus reducing the pass transistor dissipation.

Fast charging terminates when the battery terminal voltage reaches 4.2V measured by interrogation of the battery gas gauge. At the end of fast charging the battery will be charged to approximately 80% of its charge capacity.

The final phase of charging is pulsed. During pulse charging the current pulses are again set by the maximum current capability of the charger unit. The PM6650 current limit is again set to 1.2A to ensure charger voltage foldback thus minimising pass transistor dissipation. A constant on period of 250 ms is used and the terminal voltage of the battery is not permitted to exceed 4.375V during the on period of the pulse. The off time of the pulse is 125 ms. Once pulse charging is determined to be finished a period of maintenance charging commences in which the timing is 125ms on and 500 ms off. Finally the battery charging is suspended and charging is considered to be completed .

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9.3.1 Charging concept

Overview

Note: On initial inspection charging would appear to be a simple process. However, the safety requirements of Lilon cells necessitates that the phone charging system must monitor and control the process carefully. Control is achieved by means of the on board PM6650 ADC and from measurements made by a fuel gauge IC integrated into the battery.

The charging system therefore combines: phone software; PM6650 firmware and a fuel gauge system.

The battery is charged in the phone. The hardware and software is designed for Lilon with 4.2V technology. Charging is started as soon as the phone is connected to an external charger. If the phone is not switched on, then charging shall take place in the background (the customer can see this via the "Charge" symbol in the display).

With some restrictions, during normal use whilst connected to a charger, the phone will be charged. Charging commences when the charger is plugged into the phone. On plug in the charger voltage is measured to determine if it is a standard charger type (input voltage > 6.1V and <10V) or if it is a USB charger (input voltage <6.1V) if the charger fits neither category charging is immediately suspended.

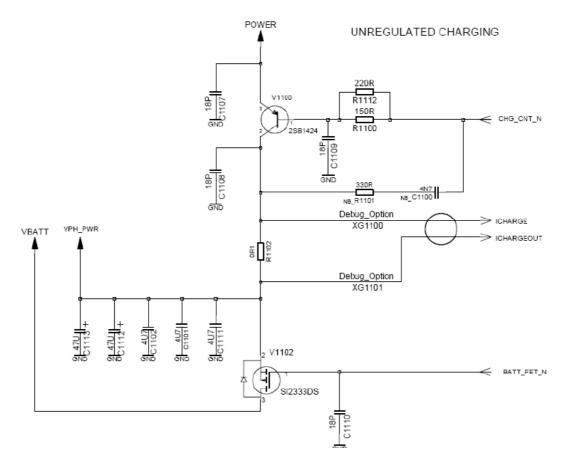
On plug in the charger is identified and if USB a phase of enumeration takes place when the USB master is interrogated to establish what current it can supply, if the charger is a wall charger then charging commences immediately. If the battery voltage is >4.1V the charging DONE state will apply and no charging takes place. If the battery voltage is <4.1V then the FAST charging mode will be invoked.

Charging is enabled via a PNP bipolar transistor (V1100) in the phone referred to as the pass transistor. This transistor operates as a switch in charging situations other than USB charging and closes the circuit from the external charger to the battery. The processor takes over the control of this switch depending on the charge level of the battery, whereby a disable function in the PM6650 hardware can override/interrupt the charging in the case of over voltage of the battery.

To control the charging process it is necessary to measure the prevailing battery temperature and the battery terminal voltage. Charging is permitted inside a temperature range of 0° C to $+50^{\circ}$ C. Charging time is dependent upon the charger and the operating mode of the phone during the charge process. With the phone in standby and assuming that the charger obeys the Normal Charger VI Envelope, then the charge current will be a maximum of 950 mA. Total charging time shall then be 1.5 hrs or less.

The charging and battery switch components are illustrated in the following figure, these components are controlled by the PM6650. The components comprise: a pass transistor (V1100) which can be operated in linear mode or driven into full saturation by the PM6650 to operate as a switch; a 0.1Ω charge current sensing resistor (R1102); a battery switch FET (V1102) which features a very low on resistance.

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Charging circuit elements controlled by the PM6650

The following signals are involved in	the battery charging process:
---------------------------------------	-------------------------------

Signal	Function
POWER	This is the supply connection to the accessory connector.
CHG_CNT_N	Drive signal from PM6650. The control for the pass transistor, V1100. Low voltage turns on the transistor.
ICHARGE	Positive current sensor input to PM6650. Used to generate feedback signal for CHG_CNT_N control.
ICHARGEOUT	Negative current sensor input to PM6650. Used to generate feedback signal for CHG_CNT_N control. Note this is the same signal as VPH_PWR - the main supply for the phone circuitry.
BATT_FET_N	Drive signal from PM6650. The control for the battery switch MOSFET, V1102. Low voltage turns on the MOSFET.
VBATT	Battery voltage monitored by PM6650. This line is also used to trickle charge the battery when it has very low voltage.

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Battery charging signals

The external charger voltage is presented on the line labelled "POWER". When using the Siemens standard charger units, it is imperative that the pass transistor is operated as a fully saturated switch and that sufficient current is drawn from the charger to guarantee voltage fold back which minimises the voltage across the pass transistor and therefore maintains the dissipation of the pass transistor within acceptably low bounds.

When operating from a USB charge source, the output voltage is limited to 5.25V maximum (no fold back) and charge current capability of the USB device is relatively low so the pass transistor can be operated in linear mode to appropriately limit the charging current.

Measurement of battery voltage, battery type and ambient temperature

Measurement of the battery terminal voltage is carried out by the MSM6250. The PM6650 routes the voltage it wants to measure to the MS6250 ADC on the AMUX_OUT line. This is the output of the analogue multiplexer in the PM6650.

A battery fuel gauge, is an in-built feature of the battery. The fuel gauge has registers which are addressed and read using a single line HDQ digital interface. Many parameters can be read from the fuel gauge including cell voltage, temperature and charge status. The fuel gauge integrated circuit is a Ti BQ27000.

During the charging process information from the PM6650/MSM6250 ADC and the battery fuel gauge are used to make decisions about the charging process.

Timing of the battery voltage measurement

In previous generations of Siemens phones, unless the battery is being charged, the measurement is made in the TX time slot. During charging it is done after the TX time slot.

Battery fuel gauge measurement timing cannot be controlled externally to the battery, hence battery status must be determined purely from battery temperature, history, and charge/discharge measurements.

Recognition of the battery type

The battery on-board protection and fuel gauge circuitry has a register addressable and read via the HDQ bus which can be used to hold battery type information.

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Trickle charging

When a Lilon battery is deeply discharged, the terminal voltage drops below 3.0V and a period of trickle charging is necessary to bring the terminal voltage up to 3.0V whereupon fast charging can commence.

The PM6650 controls the trickle charge process via an internal programmable current source, using the VBATT port. The nominal trickle charge rate for Wolf 5 is 80 mA.

The battery fuel gauge requires a cell voltage of approximately 2.8V minimum to operate properly. Therefore it is feasible that a deeply discharged cell may not be able to initially respond to fuel gauge interrogation.

The phone therefore cannot tell from this source whether a cell is installed or not. The no battery case is therefore detected by the PM6650 regulating to 4.2V on the battery pin and there being no response from the battery fuel gauge. A timer is used to ensure that a

maximum of 30mAh is delivered to the battery.

Once this has occurred if no response from the battery has been successful then an invalid cell warning is issued and charging is terminated.

Due to limitations dictated by the USB specification a device is not permitted to draw more than 100mA until after enumeration has occurred whereupon the USB master informs the slave if it can supply higher than 100mA. Unfortunately Wolf 5 must draw more than 100mA to fully boot up. If no battery power is available then this power would need to be sourced by the charger (in this case USB master). Consequently for USB if the battery is totally discharged, no additional current can be supplied to assist boot up and boot must be suspended. In this state the phone will continue to draw approximately 80mA from the USB master but will not exceed the 100mA USB specification limit. Thus if a battery if fully discharged it cannot be recharged using USB as the power source and the user must briefly connect the phone to a

standard charger until the battery has enough reserve following trickle charging and a period of fast charging to enable the boot process to succeed with USB. Normally trickle charging from a standard charger takes only a few minutes.

Normal charging (fast charge)

For battery voltages above 3.0 V and normal ambient temperature between 0°C and 50°C the battery can be charged with a charge current up to 1C. This charging mode is software controlled and starts if an accessory (charger) is detected with a supply voltage above 6.4 Volt by the PM6650. The level of charge current is only limited by the charger. The Wolf 5 normal charger is the Siemens Travel Charger which obeys the output envelope shown below.

Fast charging ceases when the fuel gauge reports that the cell voltage has reached 4.2V and the charging mode changes to pulsed current. Note that when the charging current is removed the battery terminal voltage drops back from 4.2V and at this point the battery will hold less than 100% of its fully charge capacity.

Note that the pass transistor must always be operated in full saturation and sufficient current must be drawn from the charger to ensure voltage fold back occurs thus minimising the dissipation of the input transistor. The consequence of this requirement is that the charger alone normally defines the charge current supplied to the battery. The charge current should therefore be a maximum of 950mA but could be less if a lower power charger is employed.

During fast charging the software applies an upper bound current limit of 1.2A to the charging current and monitors the power dissipation of the pass transistor limiting the maximum dissipation to 1.0W. If the power limit is exceeded the charge mode is switched to SUSPEND for 30 minutes.

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Pulsed charging

The pulsed charging mode is used to bring up the battery to maximum capacity. If the input transistor is switched off at a level of 4.2V, the battery voltage drops down. This dropdown voltage depends on the temperature, the age of the battery etc.

This final stage of charging is referred to as TOPOFF and can take place in two stages. The first stage will always occur after constant current charging has finished. This is a period of pulses with 250ms on time and 125ms off time. The PM6650 regulates to 4.2V and this first phase of pulse charging will cease either after a set number of pulse cycles during each of which the battery exceeds the 4.2V threshold (currently 16) in which case pulse charging mode will switch to maintenance or if the fuel gauge indicates charge completion with the IMIN flag in which case the charge mode proceeds to DONE and charging stops.

Towards the end of the pulsed charge TOPOFF period (before maintenance charging), on periods are skipped to reduce the duty cycle of the pulsed current and bring the average to below the taper current requirement of the fuel gauge.

Maintenance (MAINT) charging has an on time of 125ms and off time of 500ms. Maintenance charging ends either by the fuel gauge indicating charge completion with the IMIN flag or alternatively when a set number of maintenance pulses have occurred (currently 64) during each of which the battery voltage exceeds the 4.2V threshold during the off period.

Once charging is completed if the battery voltage falls below 4.1V then MAINT charge mode is restarted. If the battery voltage has fallen to below 4.0V the FAST charging mode will be invoked.

During pulse charging modes the power dissipation of the pass transistor is checked once every 60 seconds.

The PM6650 is not able to continuously monitor pass transistor dissipation but monitoring once each 60 seconds ensures that any likely developing situation is detected in time to prevent damage of the transistor.

USB charging

The PM6650 supports USB charging. USB charge voltage is specified to be in the range 4.4V to 5.25 V USB charging mode is invoked if the POWER line is measured by the PM6650 to be less than 6.1V. During USB charging only limited charging is possible. Charge current is limited to 100 mA or 500 mA depending on the capability of the USB source. The handset must initially assume the lower capability and then interrogate the device to establish if a higher charge current is possible. This process is referred to as enumeration.

Control of charge current is achieved by operating the pass transistor in linear mode. The PM6650 monitors the dissipation of the pass transistor via current and voltage measurements and can be programmed to limit the charge current in accordance with the maximum dissipation allowable for the pass transistor which is 1.0W.

On plug in of the USB master, following enumeration, if the battery voltage is determined to be >4.1V the charge mode is set to USB DONE and no charge current flows into the battery. If the battery voltage is <4.1V, then the charge mode is set to USB FAST and the maximum current allowed by the USB charger flows into the handset.

When the battery voltage reaches a level of 4.2V USB FAST charging is terminated and USB TOPOFF mode is entered. USB TOPOFF is a constant voltage charging phase where the voltage is maintained at 4.2V by the PM6650. Charging is terminated either by the fuel gauge IMIN flag indicating charge completion or when the USB TOPOFF timer expires.

Subsequently if the battery voltage falls below 4.1V the USB TOPOFF charging mode is reinstated and if due to phone current demand the voltage continues to fall and falls below 4.0V then USB FAST charge mode is entered.

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10 Audio interference and suspension of pulse charging

The low frequency pulsing of the charge current which takes place in TOPOFF charge mode makes audible interference when the phone is in a state where audio circuits are active. Hence in all such modes TOPOFF is suspended and constant current (FAST) charging becomes the only available charging mode.

In this mode if the battery voltage falls below 4.0V FAST charging will be started and will terminate when the voltage reaches 4.2V in both cases the voltage is read from the fuel gauge.

Consequently assuming that the charger can supply sufficient current to run phone activity and supply charge current, the battery voltage will be maintained to always be 4.0V or greater. If the phone is removed from the charger just before FAST charging is about to recommence then the battery will not be fully charged. However a high percentage of charge will remain at a battery voltage of 4.0V and satisfactory performance should be achieved for the user.

11 MMI

11.1 Display

11.1.1 Overview

The SXG75 display is a 2.2" QVGA (240x320) TFT display with 262 k (18 bit) color depth. The supplier for the TFT display is Epson - there is no second source. The controller is integrated with the display module.

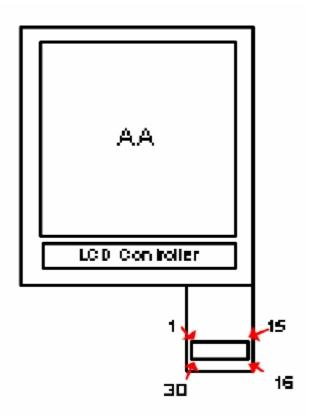
The display interface is connected to the 16-bit wide external bus interface (EBI2) of the MSM6250, which is also shared with the NAND Flash. The display I/O supply voltage (VIO) is 1.85 V (VREG_MSME) while the main display power supply (VDD) is 2.9 V (generated by regulator N2201).

The display backlight is generated by 4 white LEDs connected in series inside the display module. The LED chain is powered from a supply voltage of 18.75 V generated by a step-up converter. The brightness is controlled by a current sink circuit driven by the MSM6250 (more details below). The display is blanked at power-up and after a hardware reset.

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11.1.2 Interface display module

The display is connected to FPC socket X2201 on the main PCB via a 30-pin connector mounted on a short flex.



Orientation of LCD connector (top view)

LCD Interface signals are as follows:

X2201 Pin	LCD Function	IN/ OUT	Signal	Function
1	VLED-	I	LCD_BACKLIGHT	Series LED chain -ve
2	MODE	1	VREG_MSME	"L": 8bit parallel interface "H": 16bit parallel interface
3	LCD_CS	I	LCD2_CS_N	Chip select signal
4	LCD_A0	I	A2(20)	"L": D15 ~ D0 indicates command. "H": D15 ~ D0 indicates parameter and data.

5	RD	Ι	OE2_N	Read signal
6	WR	I	WE2_N	Write signal
7	DAT0	IO	EBI2_D(0)	D0~D7:connects to the 8/16- bit standard MPU data bus, using the 8/16-bit, bi- directional data bus
8	DAT1	10	EBI2_D(1)	EBI2 data bus
9	DAT2	10	EBI2_D(2)	EBI2 data bus
10	DAT3	10	EBI2_D(3)	EBI2 data bus
11	DAT4	10	EBI2_D(4)	EBI2 data bus
12	DAT5	10	EBI2_D(5)	EBI2 data bus
13	DAT6	10	EBI2_D(6)	EBI2 data bus
14	DAT7	10	EBI2_D(7)	EBI2 data bus
15	LCD_RESET	I	RESOUT1_N OR LCD_RST_N (D2200 OR gate)	Initialized when set to "L".
16	GND			
17	DAT15	10	EBI2_D(15)	D8~D15:connects to the 16- bit standard
				16-bit, bi-directional data bus
18	DAT14	10	EBI2_D(14)	EBI2 data bus
19	DAT13	10	EBI2_D(13)	EBI2 data bus
20	DAT12	10	EBI2_D(12)	EBI2 data bus
21	DAT11	10	EBI2_D(11)	EBI2 data bus
22	DAT10	10	EBI2_D(10)	EBI2 data bus
23	DAT9	10	EBI2_D(9)	EBI2 data bus
24	DAT8	10	EBI2_D(8)	EBI2 data bus
25	LCD_VSYNC	0	LCD_VSYNC	Synch Pin to avoid tearing effect
26	VLCD	I	2.9V from N2201	Power supply for logic
27	GND			
28	VIO	I	VREG_MSME	Power supply for I/O
29	GND			
30	VLED+	I	VREG_BCKLT	Power supply for LED backlight

LCD interface signals

11.1.3 Contrast and colour adjustment

Colour adjustment is achieved using the RGBSET command, which defines the look up table used to map the input data to the corresponding 18-bit pixel colour.

Contrast adjustment is achieved by writing an 8-bit value to the display using the WRCNTR command. The default value is 03F hex.

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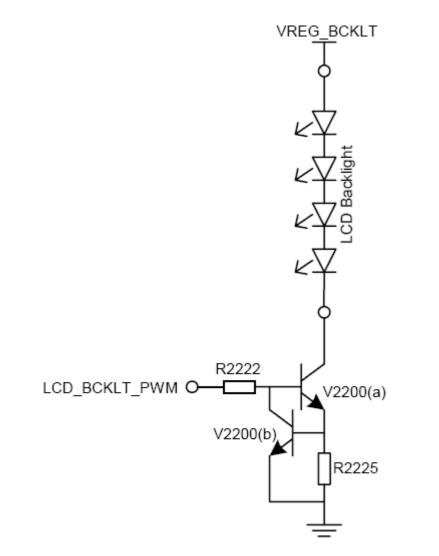
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11.1.4 Illumination

The LCD backlight is supplied by 4 white LEDs. These are connected in series to a high voltage supply at 18.75V (VREG_BCKLT). The supply is generated by switching regulator N900, and is enabled when BACKLIGHT_EN is high.

The current through the LED chain is set to 18mA using the current-limiter circuit of V2200/R2222/R2225.

The backlight brightness is varied by turning the 18mA current on and off using a pulse-width modulated switching signal LCD_BCKLT_PWM.



LCD backlight circuit

Technical Documentation TD_Repair_L3_SXG75_R1.0.pdf 01/2006 Page 53 of 73 When the LEDs are being driven, LCD_BCLKT_PWM is high, so V2200(a) is ON. Current therefore flows through R2225. When the voltage across R2225 reaches approximately 0.7V, transistor V2200(b) turns ON, and starts to turn V2200(a) OFF. An equilibrium is then reached, where the LED current is set to 0.7V/39R= 18mA.

The forward voltage of the backlight LEDs is typically 3.3V at 18mA. So the voltage seen at the collector of V2200(a) is typically (18.75-4*3.3=) 5.55V. However, due to possible tolerances on components and supply voltages, the voltage may acceptably vary between about 2.8 and 7.1V.

Backlight brightness is varied by switching LCD_BCKLT_PWM on and off using a Pulse-width modulated signal. LCD_BCKLT_PWM is generated by the General Purpose MN Timer on the MSM6250. The timer output, GP_MN (GPIO[13]) is configured to supply a Pulse-Width-Modulated signal. The LCD backlight LEDs are ON while the timer output is high, so brightness varies with the duty cycle of the timer.

The LCD_BCKLT_PWM signal also varies the brightness of the keypad backlight, so the LCD and keypad backlights will always vary in brightness together.

11.2 Keypad

The keypad assembly interfaces to the main PCB via the 16-way connector X2000. The Keypad contains 28 keys which are read as a Matrix, and a separate key which is read directly by the PM6650 in order to provide a power-on function.

11.2.1 Keypad mapping

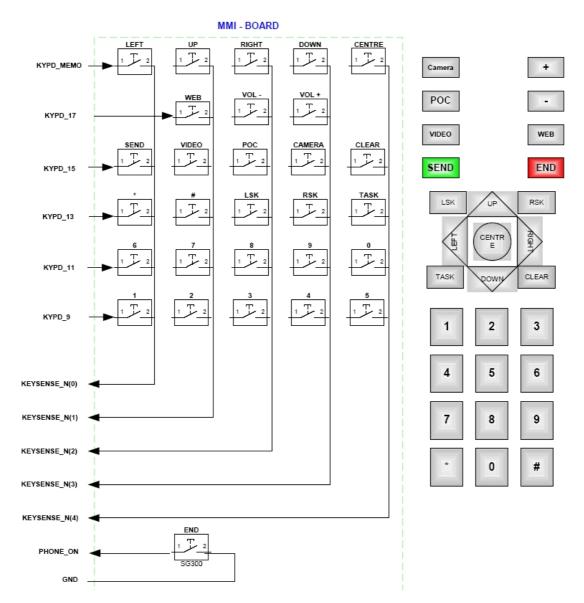
The keypad mapping and interfacing with the MSM6250 is illustrated in the following figure. This also shows the positions of the keys on the phone housing.

The Keypad is read as a matrix. The KYPD_9, KYPD_11, KYPD_13, KYPD_15 KYPD_17, and KYPD_MEMO lines are driven by the MSM6250. They are either floating (inactive), or driven low (active) one at a time. The KEYSENSE_N(0:4) lines are inputs to the MSM6250. These lines are read to detect the position of the key being pressed.

The END/Power key is connected directly to the PHONE_ON input to the PM6650 (KPDPWR_N pin). This key is read independently of the matrix to allow it to also be used to power-on the phone. The PM6650 PHONE_ON input has an internal pull-up resistor which is always active while battery voltage is available.

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Benq mobile



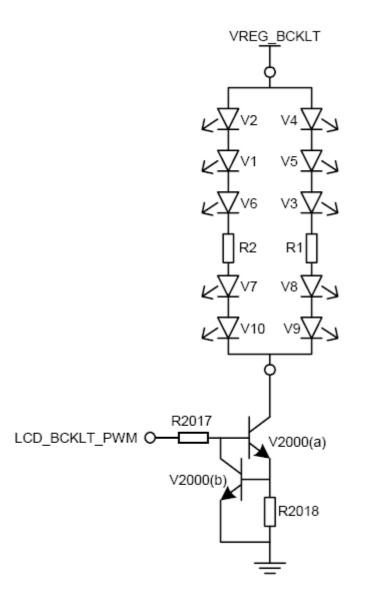
Keypad mapping

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11.2.2 Illumination

The keypad backlight is supplied by 10 white LEDs. These are arranged as two chains of 5 LEDs, both connected to a high voltage supply at 18.75V (VREG_BCKLT). The supply is generated by switching regulator N900, and is enabled when BACKLIGHT_EN is high.

The current through each LED chain is set to approximately 3mA using the current-limiter circuit of V2000/R2017/R2018. The backlight brightness is varied by turning the 6mA load current on and off using a pulse-width modulated switching signal, LCD_BCKLT_PWM.



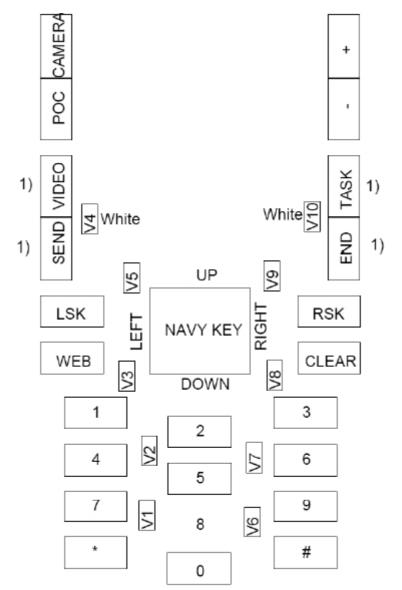
Keypad backlight

The keypad backlight is driven in the same manner as the LCD backlight. In the case of the keypad, the current is limited to (0.7V/110R =) 6.4mA.

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The voltage seen at the collector of V2000(a) is nominally 2.55V, but can vary between 0.87 and 5.43V with device tolerance.

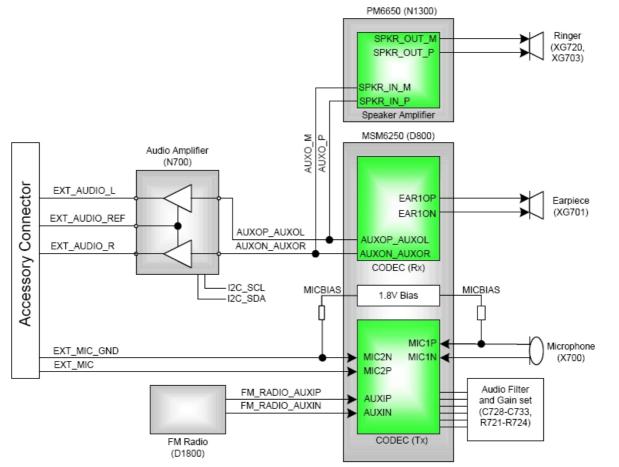
Resistors R1 and R2 in the LED chain are required to reduce the effects of any mismatch in diode forward voltage in the two chains. With 270R in each chain, if one chain has a total forward voltage difference of 0.1V, the difference in currents is 0.1/270= 0.37mA.



LED positions

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12 Acoustics



Acoustics block diagram

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12.1 Microphone, speaker and hands-free speaker

SXG75 contains an internal earpiece receiver, a hands-free/ringer speaker and a microphone. The microphone and the earpiece receiver are connected to the MSM6250 dedicated audio CODEC inputs. The hands-free speaker is connected to the output speaker driver of the PM6650 with the audio signal for the hands-free speaker provided by the auxiliary output of the MSM6250 audio CODEC. The PM6650 provides an additional series of selectable gain stages which are used to amplify the speaker output. These are varied with required volume step.

The microphone inputs can pass through an optional secondary gain stage which provides 30dB gain and additional high pass filtering. This gain stage is specified by the external components denoted above (C728-C733 & R721-R724). As well as in a call, the microphones are used for voice dialing, voice memo and the audio component of a video recording.

12.2 Audio accessories

It is possible to connect a mono or stereo headset or car-kit with microphone via the accessory connector.

The audio output of the accessory connector is provided by the auxiliary output of the MSM6250 audio CODEC which is also used as an audio source for the hands-free speaker. The audio output to the accessory connector is amplified by an external audio driver (TS4975). This device is configured using the I2C bus. The address of the device is 0xCC. The external amplifier also provides variable gain stages controllable over the I2C interface.

The microphone input from the accessories is connected to the second microphone input of the MSM6250 audio CODEC1.

A variety of wireless headsets and car kits can be used via a Bluetooth link. These bypass the above codecs and connect directly to the digital encoder and decoder stages of the MSM6250.

13 Cameras

The SXG75 has 2 integrated cameras. A CIF camera (352 x 288) from Agilent is included to support video conferencing with display of the local user image at a maximum frame rate of 15fps. The second camera is a 2 Mega pixels sensor primarily for capturing high-resolution still images but does also support video capture.

13.12Mpix camera

The Samsung 2Mega pixel camera module is mounted in socket X1901. The camera is powered from the VREG_CAM1 (2.85V) supply. This is provided from regulator N1900. The regulator is enabled when the MSM6250 control line CAM1_PWR_EN is taken high.

The camera is set-up via the I2C bus (I2C_SDA, I2C_SDA). The camera module has a 7-bit address (1000101). The 8th bit signifies a read or write operation. The I2C bus is an open-drain control, with pull-up resistors (R905, R906) to VREG_MSMP (2.6V). This bus remains active when the camera is powered down. This is allowable according to the specifications of the camera. The camera is supplied with a master clock, CAM1_DSP_CLK, from the dedicated MSM6250 interface.

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13.2 CIF camera

The CIF camera module is the ADCM-1700-1002 from Agilent. The module is mounted in socket X1900. The camera is powered from the VREG_CAM2 (2.85V) supply. This is provided from regulator N1900.

The regulator is enabled when the MSM6250 control line CAM2_PWR_EN is taken high.

The camera is also set-up via the I2C bus (I2C_SDA, I2C_SDA). The camera module address is 0x51. Again, the camera specification supports the I2C bus being active while the camera is powered-down.

13.3 Camera bus interface

Both cameras are interfaced to a single dedicated MSM6250 camera interface. The MSM6250 interface is switched between one of the two cameras with the 74ALVC16244A camera bus Switches (D1900, D1901). The bus to the Mpix camera is activated by taking the CAM1_SEL_N line low. The bus to the CIF camera is activated by taking the CAM2_SEL_N line low. Only one camera may be selected at any time.

The camera bus switches are powered from VREG_MSMP (2.6V). They also perform the function of level-shifting the 2.85V camera logic to VREG_MSMP (2.6V) levels.

The camera bus is a standard CCIR656 based interface, with signals as shown below:

Signal (MSM6250)	Signal (2MPix Camera)	Signal (CIF Camera)	Function
CAMIF_DATA(7:0)	CAM1_DATA(7:0)	CAM2_DATA(7:0)	Data output from camera
CAMIF_DSP_CLK	CAM1_DSP_CLK	CAM2_DSP_CLK	Master clock to camera
CAMIF_PCLK	CAM1_PCLK	CAM2_PCLK	Pixel clock from camera
CAMIF_VSYNC	CAM1_VS	CAM2_VS	Synchronisation pulse from camera
CAMIF_HSYNC	CAM1_HS	CAM2_HS	Synchronisation pulse from camera

13.4 Camera flash trigger

An optional flash for use with the mega pixel camera can be clipped onto the phone's accessory connector.

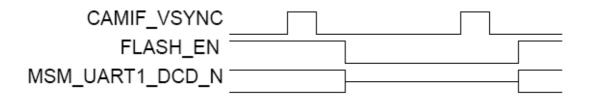
The flash accessory specification is detailed in the Clip On Flash Product Specification V0.6. The flash accessory needs to be triggered by the phone. The trigger signal for the flash accessory is generated on the DCD/CLK pin of the accessory connector. The specification emphasises the need for the flash to illuminate all camera pixels when they are all sensitive.

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01/2006 Page 60 of 73 When flash operation is required on the Samsung mega pixel camera, the VSYNC output becomes active earlier than normal. This extended pulse is used to synchronise the external flash to the time when the camera pixels are active.

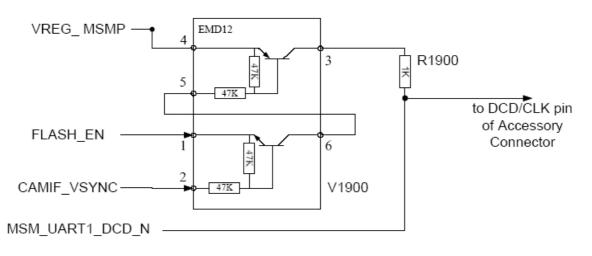
When the camera shutter is activated, The MSM6250 needs to enable one full V-sync pulse during the active camera period. So it must monitor the vertical synchronization signal CAMIF_VSYNC and enable FLASH_EN after a falling edge of CAMIF_VSYNC, as shown below. The DCD pin of UART1 (MSM_UART1_DCD_N) is also tri-stated during this period since this pin is also connected to the DCD/CLK pin of the accessory connector (flash trigger pin).



Camera flash trigger signal

The arrangement provided below allows the flash trigger (CLK/DCD) to be driven by the CAMIF_VSYNC line from the mega pixel camera whilst being controlled by the MSM6250. The clip on flash will only receive the VSYNC trigger pulse when the CAMIF_VSYNC line is high, and FLASH_EN trigger line is low.

The MSM6250 can thus enable the sync pulse by taking FLASH_EN (GPIO64) low, and setting MSM_UART1_DCD_N to tri-state.



Camera flash trigger circuit

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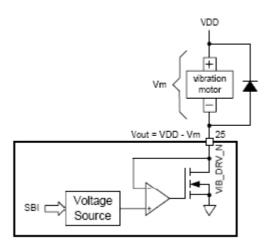
14 Vibramotor

The vibration motor is mounted in the lower case. The electrical connection to the PCB is realised with pressure contacts XG1302 and XG1303.

The vibration motor is controlled with the PM6650 vibra motor driver as illustrated below.

The vibration driver is an SBI-programmable voltage output that is referenced to VPH_PWR. When off, its output voltage is VPH_PWR.

An external diode, V1300, protects the PM6650 driver from the motor's inductive kickback. The motor is connected between VPH_PWR and pin 25 (VIB_DRV_N); the voltage across the motor is: Vm =VPH_PWR - Vout where Vout is the PM6650 voltage at pin 25. The driver (pin 25) is programmable to support motors from 1.2 to 3.1V (in 100 mV increments). The voltage is set to 2.8V for optimal performance.



Vibra driver (PM6650)

15 IrDA and fuel gauge

The IrDA transceiver and battery fuel gauge communicate with the MSM6250 using the same UART (a further spare UART is not available). So both functions are covered in this section.

15.1 IrDA transceiver

V2106 is a low power infrared data interface transceiver module. It is compatible to "IrDA - Infrared Data Association; Serial Infrared Physical Layer Specification, Version 1.3".

It supports transmission rates up to 115.2kbps (Serial IrDA).

As a Low-Power-Device, the infrared data interface has a transmission range of at least:

• 20cm to other Low-Power-Devices and

• 30cm to Standard-Devices

The viewing angle is +/-15° (resulting in 30° viewing cone). The Infrared-Interface implies a Class 1 IRLED, according to IEC 60825-1:1993+A1:1997+A2:2000.

The transceiver module is connected to UART 3 on the MSM6250. The IrDA interfaces are:

• IRDA_RXD. Data from the transceiver, connected to UART3_DP_RX_DATA/GPIO85.

• IRDA_TXD. Data to the transceiver, connected to UART3_DP_TX_DATA/ GPIO84.

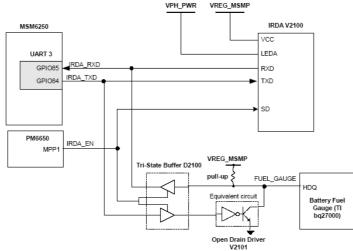
• IRDA_EN. This puts the transceiver into low-current shutdown mode when high. It also allows the transmit power to be varied. See datasheet for more details. IRDA_EN is connected to MPP1 on the PM6650. MPP1 is configured to use VREG_MSMP as a supply reference.

The IrDA transceiver digital interface is powered from VREG_MSMP. The transmit LED is powered from VPH_PWR, with a current-limited LED driver.

15.2 Battery fuel gauge and IrDA multiplexing

The battery pack contains a fuel gauge monitor from Texas Instruments (BQ27000). The fuel gauge signal is a 1-wire HDQ interface. It is multiplexed with the IrDA signal to the UART 3 port on the MSM6250.

The multiplexing of the IrDA with the fuel gauge is illustrated below.



IrDA and fuel gauge multiplexing

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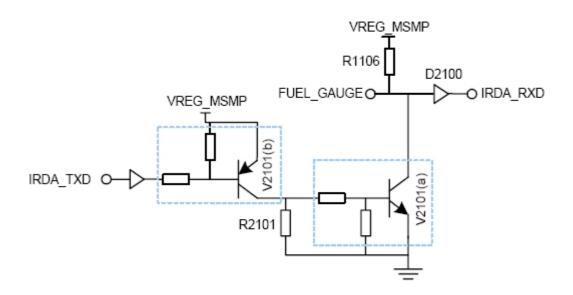
TD_Repair_L3_SXG75_R1.0.pdf

01/2006 Page 63 of 73 The MSM6250 interfaces to the fuel gauge are:

• IRDA_RXD and IRDA_TXD from UART 3. These lines can be disconnected from the fuel gauge interface via a tri-state buffer.

• IRDA_EN. The tri-state buffer is disabled when IRDA_EN is low. It is enabled when high.

The fuel gauge interface is open-drain at the battery pack. It has a pull-up (R1106) to VREG_MSMP. Since the single-wire interface is operated in an open-drain environment, an open-drain driver circuit (V2100) has been added to the IRDA_TXD interface of the fuel gauge. The fuel gauge interface is shown below:



Fuel gauge interface to UART

Data is passed from the TXD line to the fuel gauge as follows:

The FUEL_GAUGE line is pulled to VREG_MSMP by R1106.

When IRDA_TXD is taken low, the collector of V2101(b) is pulled high, which causes V2101(a) to pull FUEL_GAUGE low. This data is read by the fuel gauge. The IRDA_RXD line goes low at the same time, but this is ignored by the MSM6250.

Data is passed from the fuel gauge to the RXD line as follows:

The battery fuel gauge has an internal pulldown transistor. This pulls FUEL_GAUGE low, which in turn takes IRDA_RXD low to the MSM6250.

13. Bluetooth

SXG75 contains a BCM2004 Bluetooth RF module. The BCM2004 is powered from VREG_MSMP (2.6V) for the digital interface, and VREG_AUX2 (2.85V) for the RF/core stages. The IC contains an internal regulator which regulates VREG_AUX2 down to VDD_BT (1.8V).

The Bluetooth baseband processor is contained within the MSM6250. The dedicated Bluetooth interface between the two devices consists of a synchronous serial bus to transfer configuration and control messages, a synchronous serial bus to transfer channel data and logic control signals. Interface signal functions are described below:

Signal	Function
	Logic input from MSM6250 GPIO.
BT_ENABLE	This signal was previously used to enable the VDD_BT regulator. On the final version of Wolf 5 the control is no longer used, and the regulator is permanently enabled by pull-up resistor R1607.
BT_CLK	Logic output to MSM6250 Bluetooth interface. System clock, 12 MHz clock output derived from the BUFF_TCXO_BT reference.
BT_DATA	Logic I/O to MSM6250 Bluetooth interface. Bi-directional Tx and Rx Channel data interface signal.
BT_TX_RX_N	Logic input from MSM6250 Bluetooth interface. Multi-Purpose Pin: Rx Slot - Rx_Enable and synchronization detection; Tx Slot - Tx_En and Tx path data transfer indication.
BT_SDST	Logic input from MSM6250 Bluetooth interface. Serial interface mode control.
BT_SBDT	Logic IO to MSM6250 Bluetooth interface. Serial interface data.
BT_SBCK	Logic input from MSM6250 Bluetooth interface. Serial interface clock.
	19.2MHz master clock input.
BUFF_TCXO_BT	The TCXO clock is buffered by the single-gate inverter, D1300. The inverter is configured to operate as a linear buffer by C1332/R1310. The buffer is only enabled when the input VREG_AUX2 is high. This prevents the clock from being applied when Bluetooth is disabled.

Bluetooth module interface signals

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16 Accessory interface

16.1 Overview

A standard "Slim Lumberg" BenQ Mobile accessory connector allows approved devices to be connected to the phone. These devices include battery chargers, data transfer cables (USB or UART), camera flash and audio products (headset, car kit etc). Signals at the accessory connector are listed below:

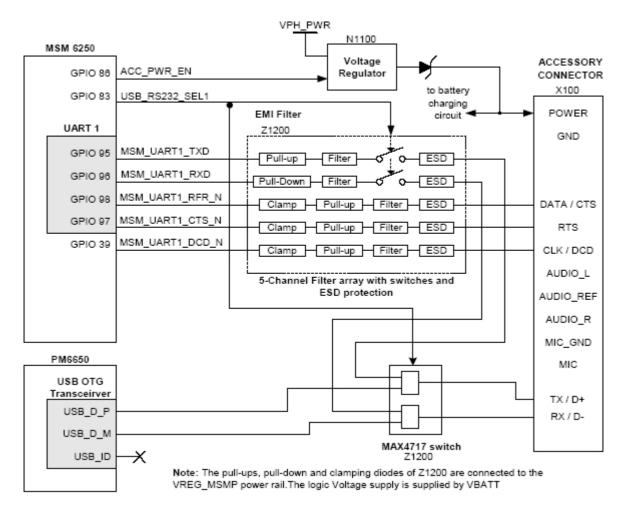
Pin	Signal	Function	Connection
1	POWER	External charging input. Supply out to accessories	Battery charger (V1100). Regulator for supply output (N1100).
2	GND	Ground	
3	ТХ	RS232 data output. D+ USB signal. Accessory recognition.	UART/USB multiplexer switch (Z1201). Then to MSM6250 UART1, or PM6650 USB driver.
4	RX	RS232 data input. D- USB signal. Accessory recognition.	UART/USB multiplexer switch (Z1201). Then to MSM6250 UART1, or PM6650 USB driver.
5	CTS	RS232 CTS output. DATA signal input and output. Accessory recognition.	UART EMI filter (Z1200). Then to MSM6250 UART1
6	RTS	RS232 RTS input. Accessory recognition.	UART EMI filter (Z1200). Then to MSM6250 UART1
7	DCD	RS232 DCD output. CLK signal output. Accessory recognition. Trigger for clip-on flash	UART EMI filter (Z1200). Then to MSM6250 UART1
8	AUDIO_L	Left audio channel output.	Audio amplifier (N700).
9	AUDIO_REF	Ground reference for audio signals.	Audio amplifier (N700).
10	AUDIO_R	Right audio channel output.	Audio amplifier (N700).
11	EXT_MIC_GND	Reference ground for microphone signal.	MSM6250 MIC2N
12	EXT_MIC	Input for external microphone.	MSM6250 MIC2P

Accessory connector interfaces

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16.2UART and USB multiplexing

On the accessory connector, the differential signals (D+ and D-) of the USB interface are multiplexed with the UART signals TX and RX.



UART/ USB multiplexing block diagram

Z1201 is a low-impedance switch which connects the accessory connector TX/RX lines either to the PM6650 USB port, or to the MSM6250 UART. Selection is controlled by the USB_RS232_SEL1 line.

All UART lines pass through the filter Z1200 (5-Channel filter array with switches and ESD protection) to protect the MSM6250.

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16.3 Connector default configuration

When no accessory is present, the accessory connector must be configured to a specific default state. This default state only applies when the phone is switched on or when the phone stays in charge mode.

The default values are shown below:

Pin	Signal	Default Level	Default Direction
1	POWER	L (Z)	off
2	GND	GND	1
3	TX	H (Z)	out (Z)
4	RX	L (Z)	in
5	CTS	H (Z)	in
6	RTS	H (Z)	in
7	DCD	H (Z)	In
8	AUDIO_L	Z	Off
9	AUDIO_REF	Z	Off
10	AUDIO_R	Z	Off
11	EXT_MIC_GN D	GND	1
12	EXT_MIC	Z	Off

Accessory connector configuration

"Z" means the driver is in high impedance state.

16.4 Accessory detection

When initially connected to SXG75, the accessory type must be determined. This is achieved by monitoring the following signals:

- MSM_UART1_RXD
- MSM_UART1_CTS_N
- MSM_UART1_RFR_N
- MSM_UART1_DCD_N

The MSM6250 must set these signals to be inputs with no internal pull-up/downs if no accessory is connected.

The RX line has an external pull-down; the CTS, RFR, and DCD lines have an external pull-up. The MSM6250 must also set the USB/UART switch to connect the TX/RX pins on the connector to the UART.

When an accessory is connected, the MSM6250 detects a change in state on one or more of the lines. The lines may be pulled high, low, or connected to the TX line in order to identify the accessory. Once the accessory is recognised, the accessory connector signals are configured appropriately.

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17 UART

The UART at the accessory connector requires the status signals CTS, RTS, and DCD to be configured as a "DCE" device. This has DCD and CTS as outputs, and RTS as an input. However, TX and RX are configured as a "DTE" device, with TX output and RX input.

UART1 on the MSM6250 is configured as a full "DTE" device, with TX and RX as above, but with DCD and CTS as inputs, and RTS (RFR) as an output. CTS and RTS (RFR) are connected directly to the UART hardware block, so their functionality cannot be changed.

DCD is connected to a GPIO pin.

To make the two compatible, connections are required as follows:

- MSM_UART1_TXD. Data output from MSM6250. Connects to TX/D+ pin.
- MSM_UART1_RXD. Data input to MSM6250. Connects to RX/D- pin.
- MSM_UART1_CTS_N. Control input to MSM6250. Connects to RTS pin.

• MSM_UART1_RFR_N. Control output from MSM6250. Connects to DATA/CTS pin.

• MSM_UART1_DCD_N. Control output from MSM6250. Connects to CLK/DCD pin.

Swapping the RTS and CTS signals as above allows these signals to be directly connected to accessories without modifying the function of UART1. The signal "switch" is made at the EMI filter Z1200.DCD becomes an output (DCE) function rather than an input. This requires a modification to the software driver. The TX and RX pins on the accessory connector are switched between USB and UART functions as required.

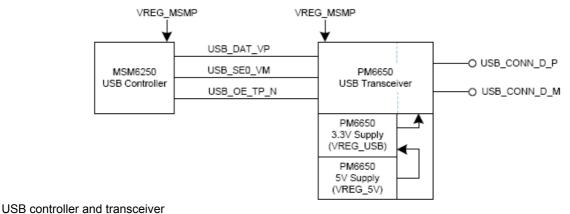
UART operation is selected by holding USB_RS232_SEL1 (GPIO83) low. The UART needs to be selected in order to detect the function of a newly connected accessory.

18 USB

USB data is supported using two pins on the accessory connector. These pins are switched between USB and UART functions as required. USB operation is selected by holding USB_RS232_SEL1 (GPIO83) high. SXG75 supports USB data transfer at 12Mbits/sec.

A separate USB power input is not provided. If a USB accessory supports charging, the supply is present at the same POWER pin as used by battery chargers. Therefore there is only one charging pass transistor (V1100). No USB power output is provided.

The MSM6250 contains a dedicated USB controller core. This interfaces to a USB transceiver core on the PM6650. The PM6650 provides the USB interface D+ and D- lines. The PM6650 USB transceiver is powered from an internal 3.3V supply. This supply is generated from the 5V boost switching supply on the PM6650. Interfaces between the controller and transceiver are shown below:



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Signal	Function	
USB_DAT_VP	Plus (+) line of the digital-differential, bi-directional USB signal to/from the MSM6250. Signal levels are translated between MSM and USB domains within the PM6650 IC.	
USB_SE0_VM	Minus (-) line of the digital-differential, bi-directional USB signal to/from the MSM6250. Signal levels are translated between MSM and USB domains within the PM6650 IC.	
USB_OE_TP_N	USB output enable signal (active LOW). Driven by MSM6250	
USB_CONN_D_P	Plus (+) line of the differential, bi-directional USB signal to/from the accessory connector.	
USB+CONN_D_M	Minus (-) line of the differential, bi-directional USB signal to/from the accessory connector.	

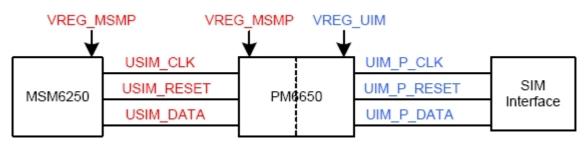
USB interface signals

19 SIM Interface

The SIM interface is powered by VREG_UIM (3.0V). SIM cards with supply voltages of 3V are supported only. 1.8V support may be made available if required (e.g. an operator's request). The SIM interface consists of the three signals UIM_P_CLK, UIM_P_RESET and UIM_P_DATA, for communication and the power-line VREG_UIM.

The SIM communication lines are managed by the MSM6250, and are level-shifted by the PM6650 to

meet VREG_UIM logic levels as shown below:



SIM interface

Z1500 provides ESD-protection and EM-compatibility, especially against RF-interference from external sources.

20 MMC interface

Reduced size MMC are supported. The card interface is supplied from VREG_AUX1 (2.85V). Card insertion is detected by the MMC_CD line. This line is an input to a MSM6250 port. The line has an external pull-up (R1400) to VREG_MSME. When a card is inserted, the MMC_CD line is pulled to ground by an internal connection in the card. This causes an interrupt to be generated to the MSM6250.

The MMC interface lines are MMC_DATA, MMC_CLK, and MMC_CMD. These lines are connected directly to MSM6250 ports. Note that MMC_DATA and MMC_CMD ports on the MSM6250 are 3 volt-tolerant.

The MMC clock is programmable by the MSM6250 and is set to 9.6 MHz (maximum possible operating frequency, when the MMC clock is derived from the 19.2MHz VCTXO).

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21 Component placement

The positions of the major components are indicated on the figures below:

